

Analyzing switched circuits to design DC-DC and DC-AC converters

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Recibido el 15 de agosto de 2005; aceptado el 26 de octubre de 2006

The purpose of this paper is to present an alternative analysis of switched circuit to design square wave generators (SWG). A SWG may be designed by using low-cost electronic components, which allows to the readers to understand how DC-DC and DC-AC converters based on the switched approach is an economic option to introduce network analysis concepts. Experimental results show that used techniques allow calculate the frequency range operation not only of the electronic components but also the effect of the power supply value on the generators' performance.

Keywords: Electric circuits; power electronics; oscillators.

El propósito de este artículo es presentar un análisis alternativo de circuitos conmutados para diseñar generadores de onda cuadrada, SWG (del Inglés Square Wave Generator). Un SWG puede ser diseñado usando componentes electrónicos de bajo costo, lo cual permite al lector comprender cómo los convertidores DC-DC y DC-AC basados en la aproximación conmutada es una opción económica para introducir conceptos del análisis de redes. Los resultados experimentales muestran que las técnicas usadas permiten calcular el rango de operación no sólo de los componentes electrónicos sino también del efecto que el valor de la fuente de alimentación tiene en el desempeño de los generadores.

Descriptores: Circuitos eléctricos; electrónica de potencia; osciladores.

PACS: 84.30.-r; 84.30.Jc; 84.30.Ng

1. Introduction

SWITCHED circuits are one of several design techniques to develop power processing applications. It is well-known that, using non-dissipative components, a boost converter is obtained by incorporating an inductor L between the DC power supply and the switched device. This type of converter is shown in Fig. 1, where the switch is operated by a clock signal, Φ . In the following explanation we shall assume that an open switch is modeled by an extremely high resistance value ($R_{OFF} \rightarrow \infty$); otherwise, the switch is closed ($R_{ON}=0\Omega$).

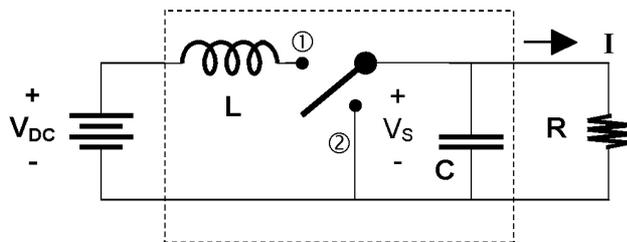


FIGURE 1. The ideal boost converter. The switch is actually a semiconductor device.

Since at any time the switch's power consumption is zero, the circuit's efficiency is ideally 100%. However, we must consider that the switch is periodically switched between nodes ① and ②, this fact is a disadvantage in the circuit because the switch is actually a field effect device (see Fig. 2). When the MOS transistor is turned on, $V_s=0$, the RC output network is grounded; otherwise, the transistor is turned off ($V_s=V_{DC}$) and the input network is connected to the output node. Apparently at any time the power consumption is zero but the accumulated electric charge when the transistor is turned on. In fact, the inverting surface connects both conducting terminals, *i.e.* the drain and the source [1]. Next, the MOS is turned off and the accumulated charge goes towards high conductive nodes (source and drain). Thus, to eliminate this parasitic signal, visualized as an output glitch, complementary MOS transistors must be used because complementary charges compensate each other. As a consequence, complementary clock signals are now required [2].

On the other hand, it is well known that switching generates undesirable harmonics. Undesirable signals may be eliminated by adding an inductor to the output network. The

circuit is shown in Fig. 2b and its transfer function is given by

$$\frac{V_{OUT}(s)}{V_s(s)} = \frac{\frac{1}{sC} \parallel R}{\frac{1}{sC} \parallel R + sL_2} = \frac{1}{CL_2} \cdot \frac{1}{s^2 + \frac{s}{RC} + \frac{1}{L_2C}}, \quad (1)$$

where s is the Laplace’s variable. From this result we obtain the output network’s resonant frequency, $\omega_0=(CL_2)^{-1/2}$. In practice, to eliminate harmonic effects the resonant frequency must be lower than the switching frequency ($\omega_0 < \omega_s$). The boost DC-DC converter shown in Fig. 2b is used in this paper as an academic vehicle to present the basics of switched circuits and also to describe how a DC-AC converter can be deduced by re-designing the output network without altering the converter’s efficiency. The reader must remember that power processing applications such as high performance and mobile applications require high efficiency because low efficiency is simply impractical.

In this paper we shall first show, in Sec. 2, how to develop square signal generators using low-cost components. The experimental results of these generators are also presented in the same section. Next, a description of the basics needed to develop a DC-AC converter is presented in Sec. 3, where some experimental results are also given. Finally, in Sec. 4 the conclusions are given.

2. Square wave generators

The simplest square wave oscillator is that labeled RC2-inverter, which gave us frequencies lower than 200 kHz. A simple modification of that oscillator is shown in Fig. 3, where an extra resistor, R_2 , is added and NAND gates are used instead of inverters. Using low-cost components, a frequency of up to 1.6 MHz is obtained when bias is as high as 9V. Because the main purpose of this paper is academic, the idea is to present basic circuits easily implemented in any electronics laboratory. A commercial 9 V battery may be used to power the oscillator shown in Fig. 3 and can be used for digital design courses, where clock generators are always welcome. Table I illustrates experimental frequencies for the RC2-NAND oscillator where just one component was varied. The result of this exercise shows that a high-bias voltage causes higher frequencies because the bias current increases. However, high voltages must be avoided to conserve the switching characteristics of gates; otherwise, internal temperature increases and there is a risk of poor performance.

As a preventive design step, lower bias may be used. In this case, the square wave generator’s frequency will be reduced because the charge and discharge times will increase. The reader must take into account that all electronic components include a data sheet where the optimum operation conditions are described by the manufacturer. In this design, the minimum bias voltage was 4V and, as was mentioned before, there was a frequency reduction as well as undesirable glitches. That response was captured by using a TDS2014 Tektronix Digital Oscilloscope (see Fig. 4).

TABLE I. Experimental frequency for the NAND-based oscillator.

R_1	56 k Ω	2.2 k Ω	165 Ω	101 Ω
R_2	10 k Ω	820 Ω	10 k Ω	10 k Ω
C_1	1 nF	1 nF	1 nF	1 nF
Frequency	45.7 kHz	208.5 kHz	1.2 MHz	1.6MHz

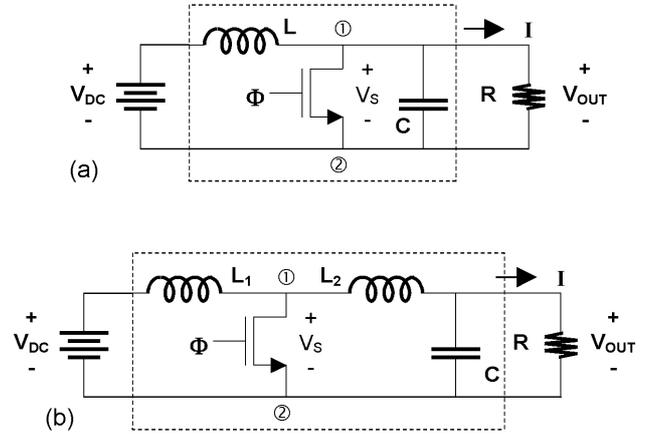


FIGURE 2. The boost converter using a MOS transistor as a non-dissipative switch (a). Including a second inductor, L_2 , harmonics are eliminated (b).

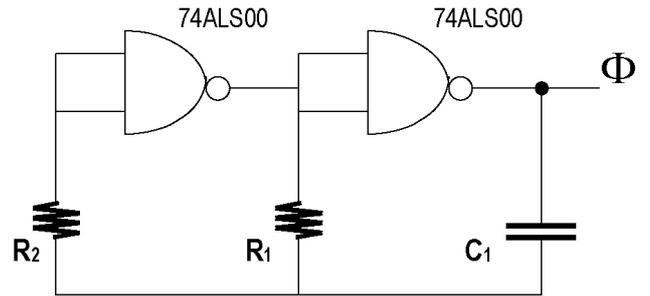


FIGURE 3. The RC2-NAND oscillator circuit.

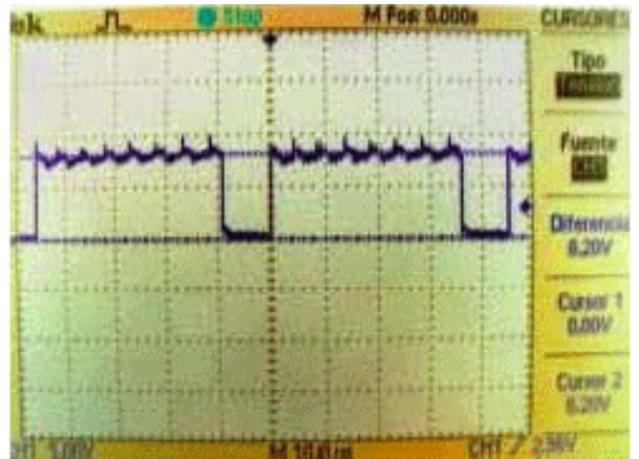


FIGURE 4. By lowering the bias voltage a spurious effect appears on the output response.

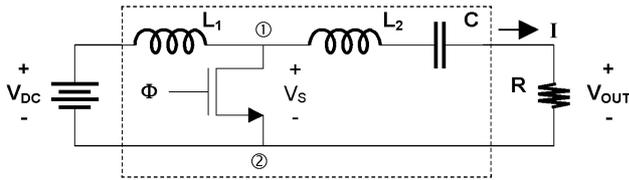


FIGURE 5. The Ideal boost converter with a L_2CR output network.

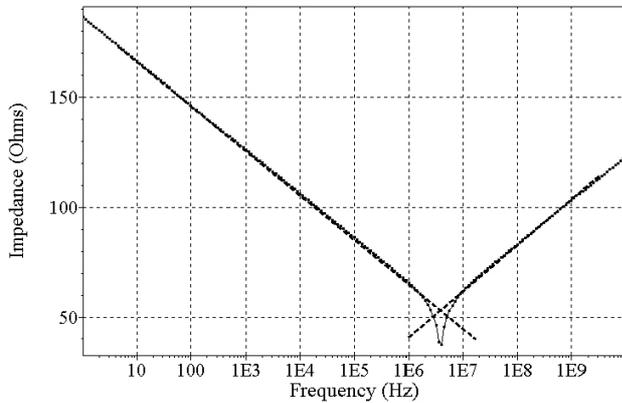


FIGURE 6. Spice simulation of the equivalent impedance versus frequency.

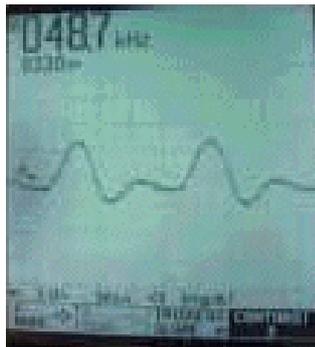


FIGURE 7. Experimental response of the pass-band filter. The curve was captured using a 123-Fluke industrial scopemeter.

3. The DC-AC converter

It was mentioned above that a low-pass filter eliminates undesirable harmonics. It was also mentioned that the filter’s resonant frequency must be lower than the sampling frequency so that the filter passes only the DC component. However, if the added filter is of the band-pass type, just one specific frequency will be measured at the output node. Figure 5 shows the converter where the capacitor is now series connected with the inductor L_2 instead of parallel connected with R .

From the point of view of network analysis, let us consider only the series LRC circuit. The equivalent impedance is

$$Z_{EQ}(s) = sL_2 + \frac{1}{sC} + R. \tag{2}$$

This result can be re-ordered as follows:

$$Z_{EQ}(s) = L_2 \frac{s^2 + \omega_0^2}{s} + R, \tag{3}$$

where ω_0 is the resonant frequency given in Sec. 1. According to this result, if the sampling frequency is equivalent to the resonant one frequency, the equivalent impedance is purely resistive because inductive and capacitive effects cancel each other. Thus it is possible to select suitable values of L_2 and C to match the output resistance. The match term refers to a proper transfer of signal from the source to a load. An interesting analysis of impedance matching can be found in Ref. 3.

As an example, Fig. 6 shows a simulation result where the impedance matching is approximately 50Ω at a frequency $\omega_0 = 2\pi(3.7\text{MHz})$ [4]. The reader must remember that the output voltage $V_{OUT}(s)$ is given by $I(s)Z_{EQ}(s)$; it is easy to demonstrate that the transfer function $V_{OUT}(s)/V_S(s)$ is band-pass type:

$$\frac{V_{OUT}(s)}{V_S(s)} = H(s) = \frac{\frac{R}{L_2}s}{s^2 + s\frac{R}{L_2} + \frac{1}{L_2C}} \tag{4}$$

Consequently, at the resonance $s = \omega_0$, the output signal would be a sinusoidal one with frequency $2\pi/T$. Fig. 7 shows experimental results of the band-pass filter when a square signal is applied. We can see that the signal’s frequency is very close to the filter’s resonant frequency; however this fact is not enough to isolate the corresponding sinusoidal signal. The latter is possible if at least two conditions are satisfied:

- there is a correct tuning frequency, and
- a high L_2RC network’s quality factor is designed

The first condition is to minimize the sensitivity of the resonant frequency to the components’ variations, while the second one is to select the needed frequency. The quality factor, commonly denoted by Q , is obtained from (4). The denominator $D(s)$ includes an independent term labeled ω_0 , while the linear term (R/L_2) is associated with the aspect ratio given by the resonant frequency and the quality factor.

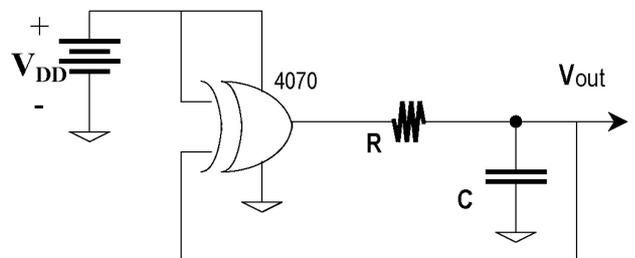


FIGURE 8. EX-OR gate is also useful in developing an oscillator circuit. The bias of the circuit presented here must satisfy the condition $3V \leq V_{DD} \leq 15V$ for correct operation.

4. Conclusions

In this paper we have introduced an analysis of basic circuits and new ways to design square wave generators. The generator is oriented to ward operating the switches of DC-DC and DC-AC converters. Experimental results verified the usefulness of the circuits presented, which are characterized by higher frequencies than the simplest RC2-inverter oscillator [5]. Next, in order to filter just one signal, the DC-DC converter's network was modified by changing the low-pass stage to a band-pass one. Here the LRC network's resonance frequency was tuned at the oscillator frequency to catch the fundamental signal. Experimental results have demonstrated that tuning is required not only to verify the LRC network's performance, but also to obtain a DC-AC converter.

The circuitry presented in this paper is low-cost and its development in any electronics laboratory, for academic purposes, is easy and highly recommended because it gives to the students the necessary background in circuits design to develop both voltage converters and oscillators circuits.

As an experimental exercise, we invite all interested people to verify that, on one hand, the oscillator circuit shown in Fig. 8 generates a quasi-sine signal. Using $V_{DD}=8$ V, $R=1$ k Ω , $C=1$ nF a frequency $f=4.7$ MHz is obtained. However, if the capacitance is 10 pF frequency increases up to 38 MHz.

On the other hand, it is possible to verify that a ring oscillator based on inverter circuits is also a square wave generator. By using digital design concepts, it is clear that an even number of inverters generates a stable circuit, *i.e.* it is not a free-running multivibrator. However, if the number of inverters is odd the circuit is unstable. In practice, that is the reason why the circuit oscillates. A disadvantage of this a circuit is

that frequency is not under the designer's control.

For those students with spice knowledge it will be easy to obtain the impedance response shown in Fig. 6 by considering that for AC analysis an input voltage source VIN is commonly described as follows:

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VIN node-1 node-2 AC 1.0
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where node-2 usually denotes the zero voltage reference, while the signal's amplitude is 1V. Next, since the network current $I(s)$ is given by $VIN/Z_{EQ}(s)$, the impedance in the frequency domain is obtained by plotting the current $I(s)$ as follows:

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.print AC '1/i(R)'
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Here $i(R)$ indicates the current driven by the resistor R. So, what about the input voltage? Finally, for those students without spice background, an evaluation spice tool can be downloaded at the website indicated in Ref. 6.

In terms of the purposes of this paper, future work includes a description about how switching components are selected and how the design components' values are calculated according to the power output needed. Because switched frequency is an additional design parameter, other oscillators will be described and analyzed. A further objective would be the design of a class-E amplifier based on commercial components.

Acknowledgments

Authors thank the anonymous reviewer for his helpful comments.

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