Basic circuits to design switched-based DC-DC converters

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The purpose of this paper is twofold. On one hand, basics on switched circuits for designing a DC-DC converter are presented and, on the other hand, power electronics definitions associated with simple electrical networks are mentioned. In the analysis of these networks, it is necessary to take into account not only converters' non-idealities but also how to minimize power losses. Since power losses may be minimized by increasing the clock frequency of switched-based converters, experimental results of basic clock generators are presented. These generators were implemented with low-cost components.

Keywords: Electric circuits; power electronics; oscillators.

El propósito de este artículo es doble. Por un lado, se presentan conceptos básicos de circuitos conmutados para diseñar un convertidor CD-CD y, por el otro, se rescatan definiciones de electrónica de potencia asociadas a redes eléctricas simples. En el análisis de esas redes es necesario tomar en cuenta no sólo las no idealidades de los convertidores sino también cómo minimizar pérdidas de potencia. Porque las pérdidas de potencia pueden ser minimizadas aumentando la frecuencia de reloj de los convertidores conmutados, se presentan resultados experimentales de generadores de reloj. Estos circuitos fueron implementados con componentes de bajo costo.

Descriptores: Circuitos eléctricos; electrónica de potencia; osciladores.

PACS: 84.30.-r; 84.30.Jc; 84.30.Ng

1. Introduction

Power dissipation is actually a limiting factor in high performance applications. Independent of application, desired performance is achieved by minimizing problems due to non-idealities. In practice, analysis, design, and optimization techniques are uncommon topics in the curricula of many academic institutions (mainly at the undergraduate level). Fortunately for those institutions, there are many simple networks that make it possible to understand undesirable effects and, more important, these networks can be implemented by using low-cost components. Thus, *uncommon topics* could be added to any curricula by including whole designs, *i.e.* from analysis to physical implementation. The objective of this paper is to present basic concepts on switched circuits using as an academic vehicle a DC-DC converter. This converter is a basic circuit in several fields of application, includinghigh performance and mobile applications . The paper is structured as follows. Section 2 presents the switched approach, various power electronics concepts, non-idealities and undesirable effects in the design of a DC-DC converter. Next, a description is given of basic circuits for developing clock generators in Sec. 3, where experimental results are also presented. Section 4 conclusions of this work.

2. The Voltage Converter

Many electronic circuits use at least a clock signal for correct operation, and they are not properly digital circuits, *i.e.* these circuits are based on the switched approach (SA). SA is used because basic components do not consume static power; however, this design technique does not take into account non-idealities of the components, thus creating problems that designers must minimize as much as possible. As a case in point, Fig. 1 shows the block diagram of a DC-DC converter, where the input power P_{IN} is provided by a voltage source and the power output P_{OUT} depends on the converter's efficiency: $\eta = P_{OUT}/P_{IN}$.

High efficiency is needed in power processing applications because converters with low efficiency are unpractical. In that sense, power loss is a measurement of the converter's efficiency:

$$P_{LOSS} = P_{OUT}\left(\frac{1}{\eta} - 1\right). \tag{1}$$

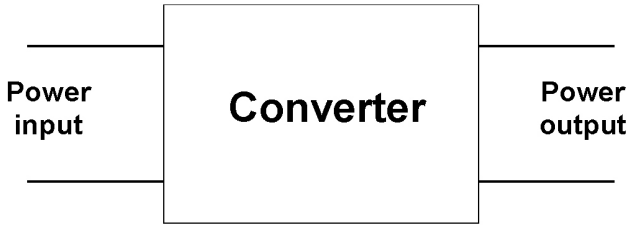

FIGURE 1. Power processing is done by the converter's electronic components.

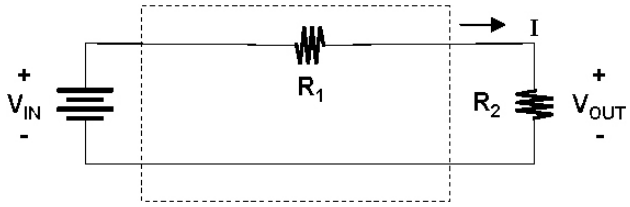

FIGURE 2. Power consumption is calculated by using the current×voltage approximation.

Figure 2 depicts the simplest DC-DC converter. By applying the Ohm's law, the total current can be estimated:

$$I = \frac{V_{IN}}{R_1 + R_2}, \tag{2}$$

hence, the output voltage is calculated by

$$V_{OUT} = \frac{R_2}{R_1 + R_2} V_{IN}. \tag{3}$$

Thus, if some application requires that$V_{OUT} = 1/2V_{IN}$, we can conclude that R_1=R_2. Next, assuming V_{IN}=5V and R_2=1.0kΩ, the current is given by Eq. (2), I=2.5mA. These data are useful for estimating power parameters: P_{IN}=(5.0V)×(2.5mA)=12.5mW, P_{OUT}=6.25mW, $\eta = 1/2$ and P_{LOSS}=P_{OUT}. In practice, this circuit is commonly used as a voltage divider; however, for low power mobile applications another DC-DC converter must be proposed [1-3].

In order to propose an alternative design option, capacitors, inductors or switching devices could be taken into account for designing a DC-DC converter. A proposal including a switch is shown in Fig. 3a, where ideally V_S=V_{IN} when the switch is turned on; elsewhere V_S=0, so that at any time the power consumption is zero. It is important to underline the fact that ideal switches present an on-resistance R_{ON}=0Ω [4]. However, it behaves as an open circuit during the off state. In practice switching devices are operated with a clock signal of period **T** (=1/f_s). The period allows for recovery ofthe duty cycle of the signal by applying Fourier analysis, *i.e.* the DC component of a periodic signal (see Fig. 3b) is equivalent to its average value:

$$V_s = \frac{1}{2} \cdot \frac{1}{L} \int_{-L/2}^{L/2} V_{IN} dt = \frac{V_{IN}}{2} \tag{4}$$

This result assumes that the signal's amplitude is equivalent to V_{IN}. As we have seen, the switch changes the DC voltage by a factor D=1/2. This is the signal's so-called duty cycle.

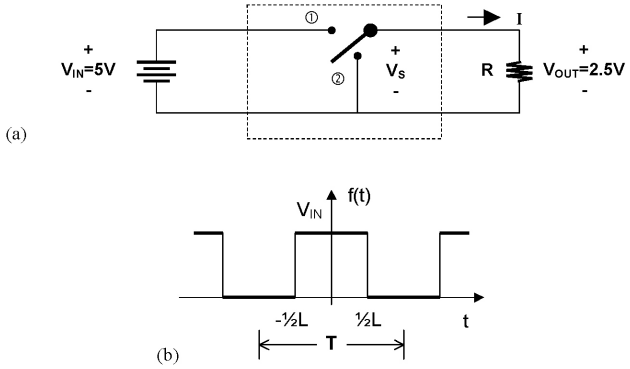

FIGURE 3. The voltage V_s=V_{IN} means that the on-resistance of the switch, R_{ON}, is zero (a); square signal example with period **T**=2L (b).

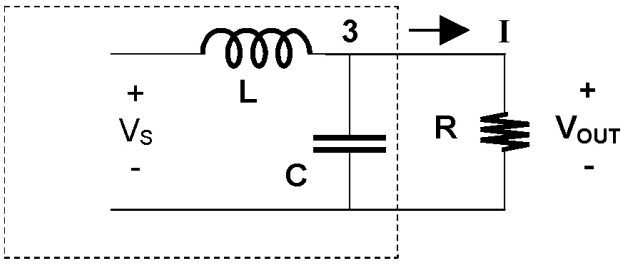

FIGURE 4. To minimize harmonic effects, the resonance frequency must satisfy $\omega_0 ¡ \omega_s$, where ω_s=$2\pi f_s$).

The duty cycle is another important parameter because it defines the interval of time in which the signal's amplitude is equivalent to V_{IN}. Let us suppose that we wish to convert the input voltage V_{IN}=5V shown in Fig. 3a to another output value, for example V_{OUT}=1.25V. From Eq. (4) we can see that a duty cycle D=1/4 satisfies this requirement, *i.e.* the integration limits are $\pm 1/4$ L.

In practice, the SA generates undesirable high frequency signals called harmonics. In order to reduce harmonics, a low-pass filter must be used. Figure 4 depicts a LC filter where the Laplace domain open loop voltage at the common node (labeled **3**) is given by

$$\frac{V_3(s)}{V_s(s)} = \frac{\frac{1}{sC}}{\frac{1}{sC} + sL} = \frac{1}{1 + s^2 CL} = \frac{1}{CL} \cdot \frac{1}{\omega_0^2 + s^2} \tag{5}$$

where ω_0=$(CL)^{-1/2}$ is the resonance frequency, while Z_L=Ls and Z_C=$(sC)^{-1}$ were used for modeling the impedance of the inductor and capacitor, respectively. Equation (5) presents the required low-pass characteristics; however, resistor R must be taken into account because it is also connected at the same node. In this case the transfer function H(s) is given by

$$\frac{V_{OUT}(s)}{V_s(s)} = H(s) = \frac{\frac{1}{sC} \| R}{\frac{1}{sC} \| R + sL} = \frac{1}{CL} \cdot \frac{1}{s^2 + \frac{s}{RC} + \frac{1}{LC}}. \tag{6}$$

As we can see, the filter actually presents a 2^{nd} order low-pass characteristic, where the impedance of the resistors **R**

affects the filter's quality factor only. This sounds good, because the resonance frequency is just a function of the LC network as was found before.

Since passive components and switches are non-ideal network components, the efficiency is lower than 100%. As we shall see, switching frequency ω_s plays a basic role not only in the dynamic power consumption but also for calculating the passive component values.

A. Boost Converter

This converter includes an inductor L between the DC voltage source and the switching devic, as Fig. 5 shows. At this point we can see, on one hand, how many components are substituting for the resistor R_1 shown in Fig. 2 and, on the other hand, we can not forget that the main objective is to minimize power loss. The advantage of the boost converter is that voltages higher than V_{IN} can be obtained, whereas the disadvantage is related to inductors because of their weight, size and volume.

The LC-based boost converter is not the only proposal for reducing power loss. Figure 6a shows a purely capacitive boost converter, which works with complementary clock signals, Φ_1 and Φ_2. In order to analyze how this converter works, we shall assume that an open switch models an *open circuit* ($R_{OFF} \rightarrow \infty$), otherwise the switch is closed, R_{ON}=0Ω. Then, if Φ_1="**1**" (Φ_2="**0**"), the equivalent circuit is shown in Fig. 6b. We can see that the voltage drop in C_1 is equal to V_{DC} while C_2 keeps its original charge. Next, Φ_2="**1**" (Φ_1="**0**") and the output voltage is V_{DC} plus the voltage drop in C_1 (see Fig. 6c). In other words, the output voltage is equivalent to the series connection of two voltage sources. Consequently, this circuit is ideally a voltage multiplier or a 2× circuit. Figure 7 shows simulation results of this circuit, where V_{DC}=1.5V was proposed. From these results some conclusions are obtained:

- there is a settling time S_t = 250μs.
- the output voltage is of the order of 2.8V, and
- the voltage ratio is A_v=V_{OUT}/V_{DC}=1.86.

So why is the capacitive DC-DC converter not a 2× circuit? In the ideal analysis, neither current I nor R_{ON} ($> 0\Omega$) were taken into account. In other words, voltage loss a is function of the charge and discharge time of capacitors. Both

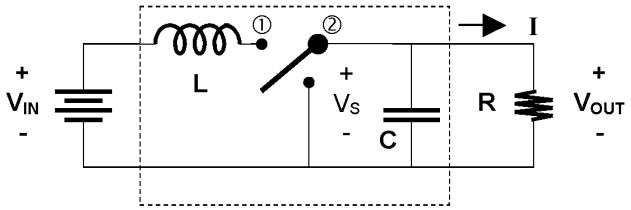

FIGURE 5. The boost converter. In practice the switch is a semiconductor device.

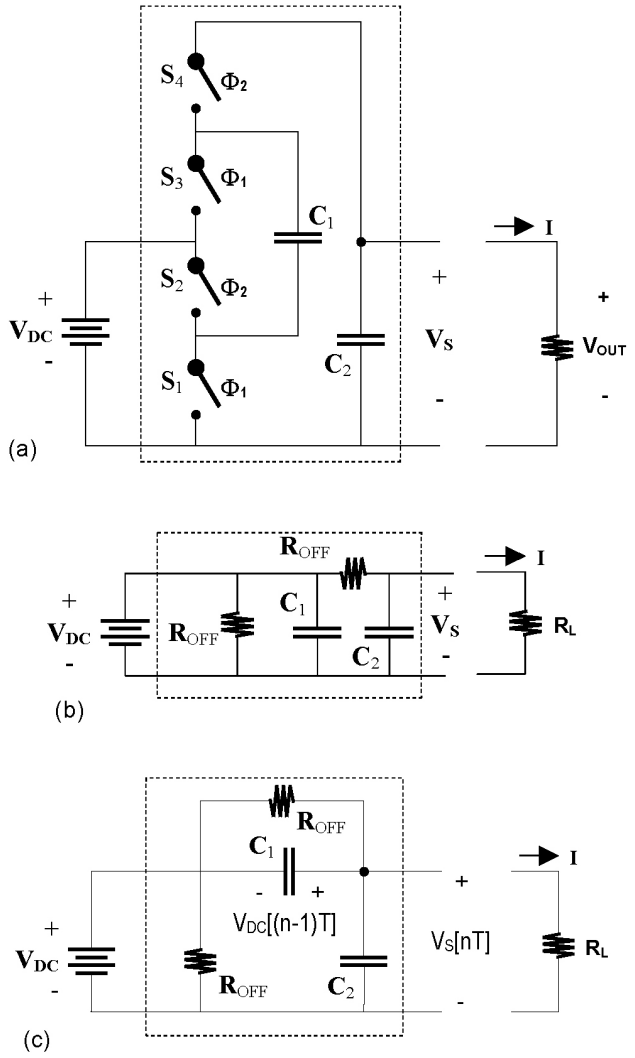

FIGURE 6. Capacitive boost converter (a); equivalent circuit at Φ_1="**1**" (b); during the time Φ_2="**1**" an ideal 2× circuit is obtained (c).

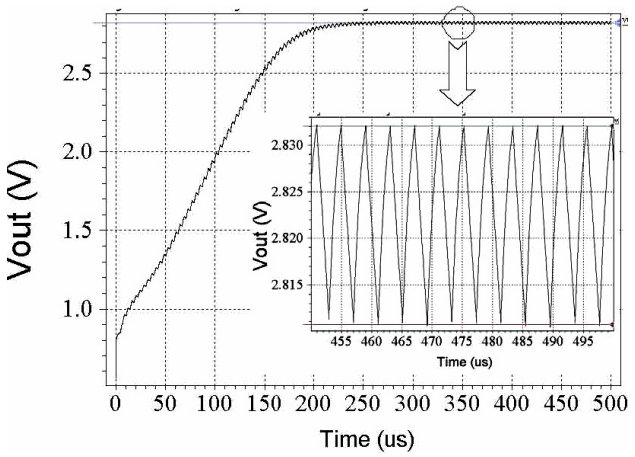

FIGURE 7. Simulation result of the 2× circuit with V_{DC}=1.5V, R_{ON}=20Ω, C=0.1μF and I=1mA.

parameters involve a product R'C, where C is either C_1 or C_2 and R' is usually associated to the switches' on-resistance. Simulation results were obtained by proposing a switch based on a MOS transistor with an on-resistance R_{ON}=20Ω. In order to present an analytical equation for modeling the output voltage as a function of both the current I and the on-resistance R_{ON}, we can use the result given by Vargas in Ref. 5. This result [see Eq. (7)] was obtained by assuming that C_1=C_2=C and taking into account the charge/discharge time. That is the reason why Eq. (7) includes two constant times, T_2 and T_3. The first constant time is the time in which C_2 delivers charge to the load, while the second one is the time in which C_2 gets charge from capacitor C_1. From that equation we can verify that if $R_{ON} \rightarrow 0$, Eq. (7) reduces to $V_{OUT}(0^+)$=$2V_{DC} - 1/2$IT/C. It is important to note that Eq. (7) models the final value of V_{OUT} only. Thus it is not possible to calculate the settling time. On the other hand, since the on-resistance can by approximated by $R_{ON} \approx$T/C [6], the boost converter is a true 2× circuit by proposing T→ 0, or equivalently by increasing the clock frequency as much as possible. Unfortunately, the ripple at the output voltage depends on the clock frequency [5]. Hence, the final output voltage and the ripple's amplitude is a design trade-off. So how much can the clock frequency can be increased?

B. Results review

As was mentioned earlier the simplest DC-DC converter is the resistive one. The efficiency of that circuit is poor, however, because of the high power loss mainly for portable applications. Thus, in order to minimize power loss, a switched-based LC network was proposed. These components, capacitors and inductors, are commonly used in electronic design. However, the weight, size and volume of inductors are disadvantages that we must evaluate before adding them as part of a design. On the other hand, capacitors do not suffer from the inductor's disadvantages. Hence, switched-capacitor circuits are a useful design option.

As we have seen, capacitive DC-DC converters suffer from voltage loss because of the on-resistance of the switches. In order to face such non-ideality, switches with low on-resistance should be the designer's choice. Alternatively, to minimize voltage loss, the designer must remember that the clock period is under one's own control. According to that, since a clock generator is a basic circuit for operating switched systems, the analysis of some simple topologies is mandatory.

3. Square Wave Circuits

There are several economical ways to develop this class of circuits by using well-known components. The simplest clock generator is the so-called ring oscillator (RO), which is composed of a chain of **n**=(2**k**+1) NOT gates, where **k** is a natural number [**7**]. The advantage of ROs is their simplicity, whereas the disadvantage is the oscillation frequency f_{osc}, which is not under the designer's control but the gates number. The latter means that f_{osc} is a function of **n**. Another oscillating scheme that can also be implemented in all teaching laboratories is shown in Fig. 8a. The period T (=1/f_{osc}) of this circuit, hereafter labeled RC2NOT, is a function of the time constant RC. For example, a 23.3 kHz square signal is obtained by choosing R=4.7kΩ, C=4.7nF, and a power supply V_{DC}=9V. In order to increase the oscillation frequency, lower capacitance/resistance values can be proposed. In this case, the newest constant time will be lower than (4.7kΩ)(4.7nF)=22×10^{-12} sec. Since these circuits are powered with the help of a source V_{DC}, the signal amplitude is equivalent to V_{DC}. Next, if higher frequencies are generated, there is another trade-off to be evaluated: the amplitude of the signal is lower than V_{DC}. As an example of that, we can choose R=330Ω and C=4.7nF; hence the frequency is f_{osc}=196.6 kHz, whereas the amplitude is as low as V_{MIN}=1.5V, *i.e.* the voltage ratio is $A_v = {}^1/_6$. For battery powered systems, a low voltage ratio means power loss, otherwise such signal amplitude is still useful for operating switches. For example, if the switch shown in Fig. 6 is an n-type MOS transistor, the amplitude V_{MIN} is enough to drive it, because the threshold voltage is lower than 1V [8]. On the other hand, the operation of the circuit shown in Fig. 6 requires complementary clock signals. That means another

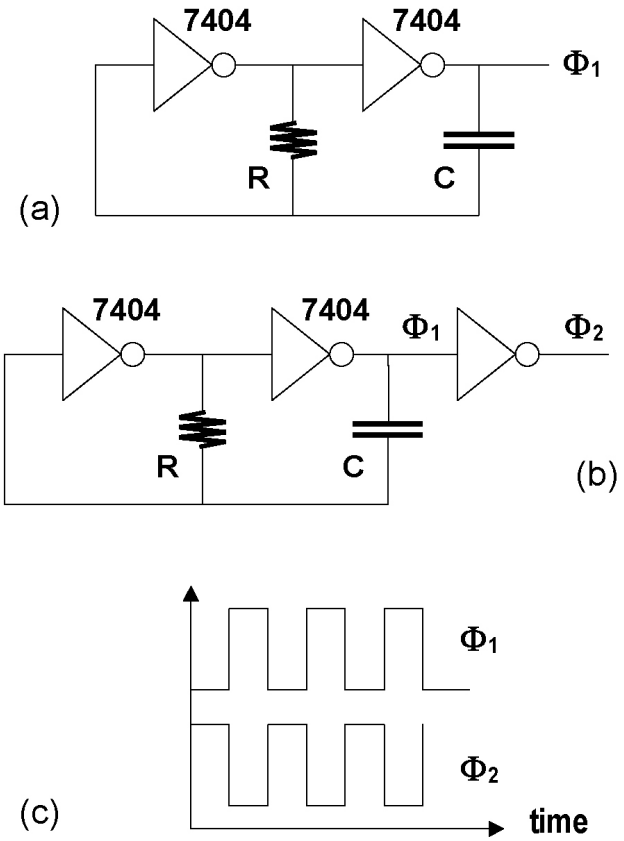

FIGURE 8. The RC2NOT signal generator (a); complementary clock phases, Φ_1 and Φ_2 (b); both signals in the time domain (c).

NOT gate must be added to satisfy that requirement. The newest circuit is depicted in Fig. 8b, while Fig. 8c shows both signals. The latter follows an illustrative purpose, and no DC level are assumed.

$$V_{OUT} = 2V_{DC} - \frac{I}{2C}\left[T + T_2\left(1 - e^{-T_2/R_{ON}C}\right)\right] \times \left(\frac{3}{2} + e^{-T/4R_{ON}C}\right) - I\left[\frac{T_3}{C}\left(1 + e^{-T/4R_{ON}C}\right) - 2R_{ON}\left(3 + e^{-T_3/R_{ON}C}\right)\frac{T_3}{T}\right] \quad (7)$$

Circuits using complementary signals suffer power loss if some cautions are omitted. For example, when signal Φ_1 goes from **1** to **0**, Φ_2 operates from **0** to **1**; that means there is a time Δt in which both switches are turned on, *i.e.* the switch's on-resistance consumes power. To achieve power savings that minimize power losses, a non-overlap signals generator must be designed. One proposal is shown in Fig. 9, where the input signal could be the response given by the RC2NOT oscillator. Here, the output NOT gates introduce a non-overlap region because of the gates' delay.

Figure 10 shows experimental results of the circuit shown in Fig. 9, where the response was captured by using a TDS2014 Tektronix Digital Oscilloscope. From this figure nothing can be said about the non-overlap region; however, by doing a close-up (see Fig. 11), such, region can be identified. In practice, a non-overlap region can be obtained by knowing the importance of the gate's logic threshold voltage, V_{LTH}. That parameter, associated with a NOT gate, is approximately $1/2V_{DC}$ because of symmetry considerations. In fact, at the input voltage equal to $1/2V_{DC}$, the NOT gate drives its maximum current. This is the reason why reducing VLTH save power is done.

Figure 11a shows the logical transition of both signals (Φ_1: **1**→**0**, Φ_2: **0**→**1**), where it is easy to see that $V_{THL} < 1/2V_{DC}$. This performance indicates that one switch is first turned off and then the second switch is turned on. The same is true for the next logic transitions shown in Fig. 11b (Φ_1: **0**→**1**, Φ_2: **1**→**0**), where V_{LTH} is lower than $1/2V_{DC}$. Hence, a non-overlap signal generator certainly saves power.

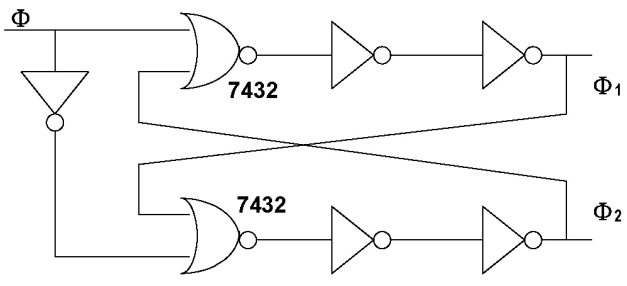

FIGURE 9. Basic circuit for generating a non-overlap region between clock signals.

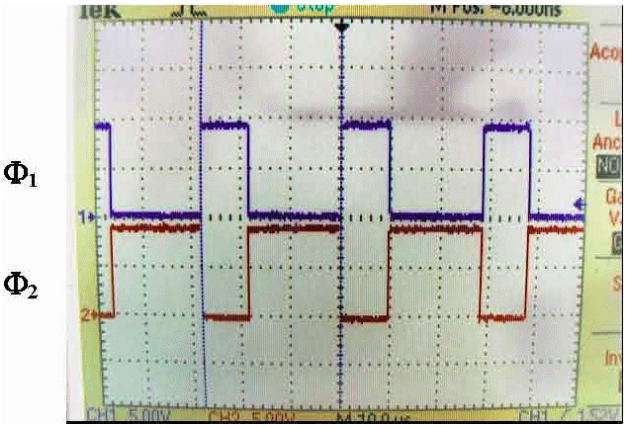

FIGURE 10. Experimental response of the circuit shown in Fig. 10, where f_{osc}=35.7 kHz and V_{DC}=10V.

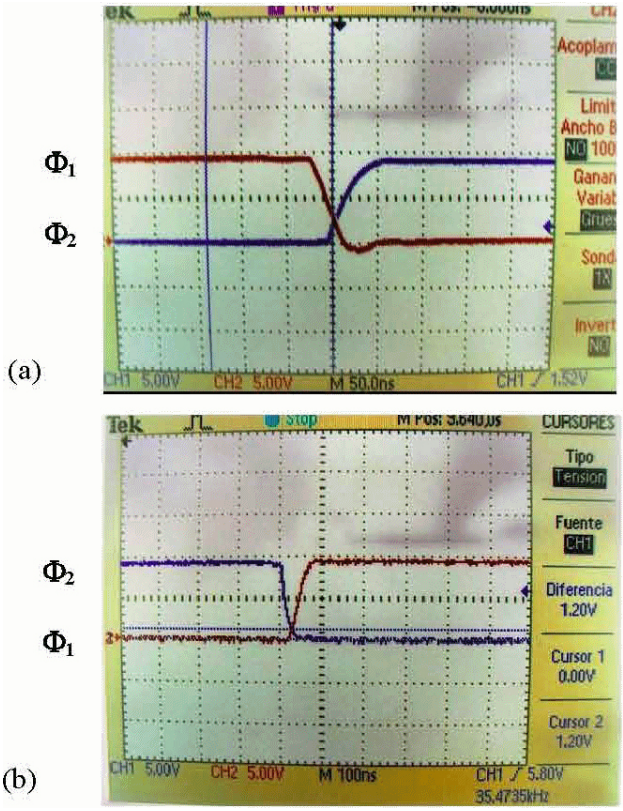

FIGURE 11. The non-overlap regions between signals. Here R=330Ω and C=22nF were used.

A. Laboratory

As we have seen, the frequency of the RC2NOT oscillator was as high as 196.6 kHz for a power supply V_{DC}=9V. An additional activity for the reader is the circuit shown in Fig. 12, where NAND gates are used. This circuit, labeled hereafter RC2NAND, generates a clock signal up to 1.6 MHz for a power supply V_{DC}=9V. Also, the reader must test the design of a ring oscillator by varying the number of NOT gates. In this case, experimental data will indicate the frequency value as a function of **n**. In fact, different frequency values are obtained by proposing other V_{DC} values.

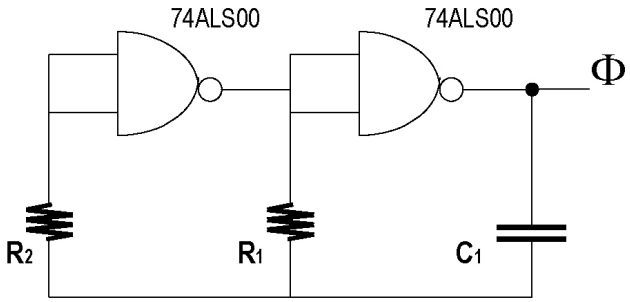

FIGURE 12. The RC2NAND oscillator circuit.

4. Conclusions

As we have seen, circuits based on the switched approach use a clock generator. Throughout this paper, non-idealities associated with DC-DC converters were discussed in order to underline advantages/disadvantages between different DC-DC topologies. Disadvantages, on one hand, are related to both voltage and power loss because of resistive components. On the other hand, in order to save power, resistors have been substituted by alternative components, switches and capacitors being the best choice. However, switches present intrinsic resistance that also represents power losses; thus, in looking for solutions to face such non-ideality, increasing the clock frequency f_{osc} was a proposed design option.

Low-cost components, including batteries, were used to implement simple clock generators. These circuits are non-complex and can be implemented in any electronics laboratory. Since physical implementation allows the trainees to verify design specifications and also take into account design constrain, it is possible introduce uncommon topics in academic curricula in order to introduce analysis, design and optimization techniques. According to this, authors in this paper have used a DC-DC converter as a vehicle for presenting basics on switched techniques and mentioning some power electronics definitions.

A whole design is not a individual work but team work. However, throughout this paper non-idealities were underlined in order to analyze the efficiency of the converter as well as to eliminate components that induce power loss. Once the importance of the clock frequency in the design of high performance circuits has been analyzed, future work includes an analysis about how to select switching devices and why such a choice introduces additional non-idealities effects.

Finally, readers should implement clock generators presented here and propose other circuits by taking into account the fact that a clock generator works under a couple of requirements: feedback positively an inverting gain stage. According to this, simple analog circuits can also be used for designing oscillator circuits.

Acknowledgments

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