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Detector control system for forward diffractive detector

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The proposal of this work is an update on the development of a control system (DCS, Detector Control System) for the new Forward Diffractive Detector (FDD) and its integration in the ALICE experiment, according to the rules of the new Online-Offline (O^2) infrastructure for Run 3 of the LHC, by using the SCADA system (Supervisory Control and Data Acquisition) called WinCC-OA®. This proposal will allow the DCS of FDD detector to have an optimal performance in the physical data acquisition runs.

Keywords: ALICE; FIT; FDD; DCS.

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1. Introduction

ALICE (A Large Ion Collider Experiment) is a heavy-ion collision experiment in the Large Hadron Collider (LHC) at CERN (European Organization for Nuclear Research). It is designed to study the physics of strongly interacting matter, in particular the properties of Quark-Gluon Plasma (QGP) by collisions of proton-proton (p-p), lead-lead (Pb-Pb), and proton-lead (p-Pb) at high energies [1]. ALICE comprises various detectors and is currently under upgrade for Run 3 [2]. The crucial requirements imposed on all detectors are the DAQ and computing infrastructure to improve collision rate handling capabilities. The interaction rates will increase by a factor of 100; therefore, the data from the detectors must be processed immediately by the O^2 system during collisions [3]. As part of this upgrade, ALICE Diffractive (AD) [4] was replaced by FDD, and it is part of ALICE's Fast Interaction Trigger (FIT) project [5]. Therefore, upgrading the AD to FDD detector implies developing a new control system (FDD-DCS).

2. FIT-FDD

2.1. Fast interaction trigger

The FIT detector serves as an interaction trigger, online luminometer, initial indicator of the vertex position, and the forward multiplicity counter [5]. The FDD detector is part of one of the three sub-detectors that make up ALICE's FIT project, together with FT0 and FV0 detectors (Fig. 1). FDD will contribute with the measurements of the time and luminosity of collisions. It will be used mainly for the study of diffractive physics.

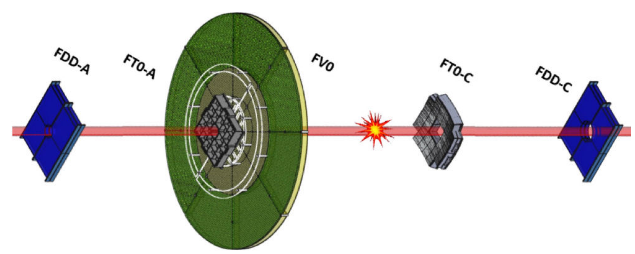

FIGURE 1. Fast Interaction Trigger sub-detectors.

2.2. Forward diffractive detector

The forward regions (A and C sides) of the ALICE cavern (Fig. 2) were assigned to the FDD detector [6] for operation during Run 3 of the Large Hadron Collider (LHC). The FDD detector consists of two sub-detectors called FDD-A and FDD-C (Fig. 3). Each of them includes two detector layers, and each layer consists of four scintillator modules arranged around the LHC beam pipe to collect the particles emerging during collisions. The FDD-A and FDD-C designations refer to the installation positions at both ends of the ALICE site concerning the interaction point (IP).

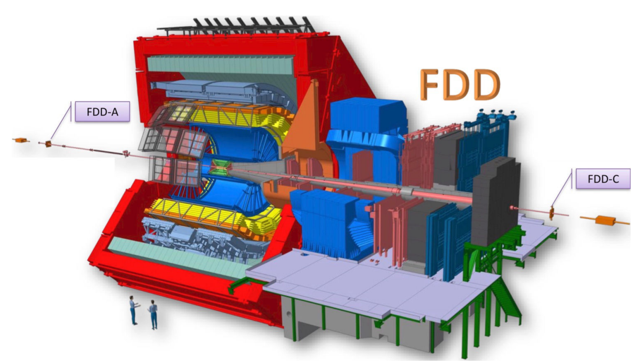

FIGURE 2. FDD-A and FDD-C sub-detectors in ALICE.

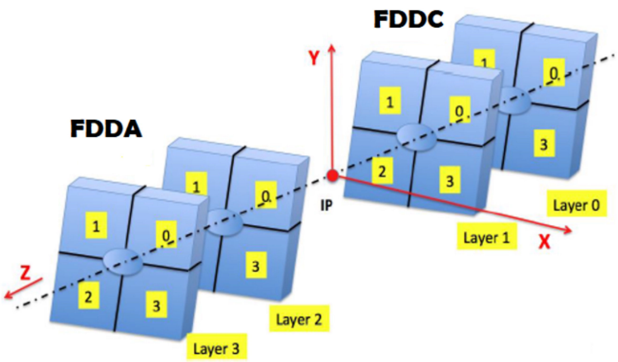

FIGURE 3. FDD-A and FDD-C sub-detectors layers.

2.3. FDD installation in ALICE

Both sub-detectors: FDD-C and FDD-A, were built and in-stalled on the C and A sides of ALICE's cavern, respectively, including the eight photomultipliers (PMTs) required to convert the light to an electrical signal from each sub-detector. Said in-stallation took place during 2021 [7].

2.4. Online-offline

One of the main updates that are being carried out at the LHC during the Long Shutdown number 2 (LS2) is the Online-Offline infrastructure that will be used in Run 3, since the high-precision measurements that will be carried out in the detectors of ALICE, CMS, ATLAS and LHCb experiments will be at a higher collision rate and luminosity than the previous runs (Runs 1 and 2). Therefore, the data from the detectors must be processed immediately online during collisions to reduce the costs and requirements of the computer systems to process and archive such data generated during collisions [3].

2.5. Detector control system

The DCS is one of the most critical software systems that allows the operation of High Energy Physics experiments (HEP). All equipment and devices that make up detectors' subsystems must be integrated into DCS's software to allow their control, monitoring, and configuration [8,9]. Upgrading the existing detectors or installing new detectors with online-offline processing capacities implies to develop new control systems (DCS).

2.6. FDD Electronics

For FDD, two A7030DP high voltage boards are used to power the 16 PMTs, that will transform the optical signals that comes from FDD to analog electrical signals. Two Processor Modules (PMs) boards are used for FDD, one for each sub-detector (FDD-A and FDD-C), which processes the analog signals from the PMTs. FDD has only one Trigger and Clock Module (TCM) board, that enables the reading of data from the two PMs. Each PM is connected to the dedicated TCM via an HDMI cable to transmit pre-trigger data, slow-control data and LHC clock distribution. The commands, configuration data, and status data are sent from the ALICE control system to the TCMs via a 1 Gb Ethernet optical link using an IPbus (UDP based protocol) [10]. Laser pulses are used for time and amplitude calibration, as well as monitoring of aging and radiation damage of the FDD sub-detectors. Finally, the Control Server communicates the control and status parameters between each FIT subsystem's TCM and WinCC-OA® software as a part of the DCS.

3. Control hierarchy for FDD

3.1. Software architecture

The DCS will monitor the status of the FDD-A and FDD-C sub-detectors. It will also supervise the electronics present in such experiment, for instance: PM, TCM, and the infrastructure of the experiment, such as the power supply devices and the temperature of the crates where various electronic devices are located.

3.2. Hardware architecture

The FDD-DCS has the following hardware architecture (Fig. 4):

- The supervision layer consists of Operator Nodes (ON) that provide the user interfaces to the operators and it is located in ALICE control room.
- The process control layer consists of Worker Nodes (WN), PLCs and PLC-like devices that interface to the experiment equipment. It is located in the Counting Room (CR).
- The field layer comprises field devices such as power supplies, field bus nodes, sensors, actuators, and more. This layer is located in the ALICE cavern.

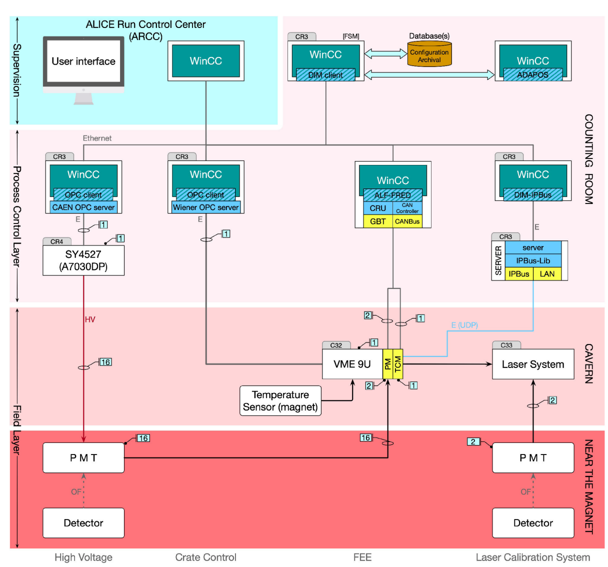

FIGURE 4. FDD-DCS hardware architecture.

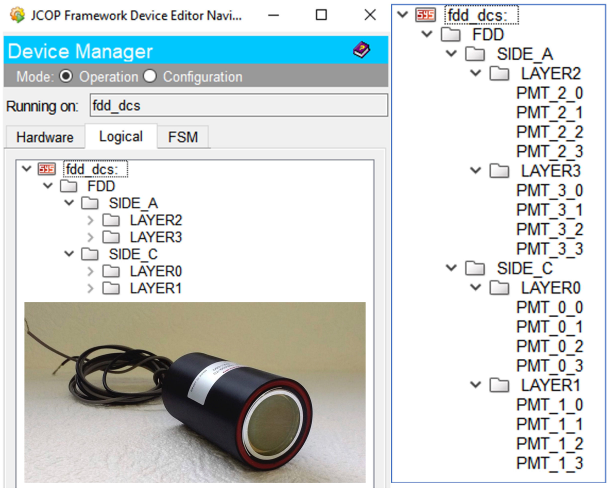

FIGURE 5. PMT logical hierarchy for FDD-DCS.

3.3. Hardware of the FDD-DCS

The hierarchy of the CAEN A7030DP high voltage boards used to power the PMTs was configured in the FDD-DCS using the SCADA system. Such CAEN boards are inserted in the CAEN crate SY4527 located in Counting Room 4 (CR4).

3.4. Logical of the FDD-DCS

Another part of the development of the control system that was done is to configure the logical hierarchy corresponding to the PMTs of the FDD detector on side A and side C of the cavern of the ALICE experiment. This is necessary for the control system to identify the 16 PMTs (Fig. 5) and read the data from such PMTs during collisions.

3.5. Finite state machine of the FDD-DCS

The hierarchy of Finite State Machines (FSM) was defined for the upper node and the control nodes of the FDD detector on both sides, as well as that of the PMTs. This is required for the control system to monitor the status of the FDD-A and FDD-C sub-detectors, as well as send ON (SWITCH ON) or OFF (SWITCH OFF) commands to the 16 PMTs [11].

4. User interface and alarms

4.1. FDD-DCS main panel

Using the WinCC-OA® software, the first version of the main panel of the FDD-DCS has been developed (Fig. 6). The DCS must have a main control panel to be managed by an operator of the ALICE experiment's central control system to monitor the detector's general status during collisions.

4.2. FDD-A and FDD-C sub-panels

The first version of the panel to monitor and control the A and C side of the FDD detector was also developed. The main panel of DCS must have sub-panels of control that allow the operator to obtain more details of the status of the different parts of the detector and control such parts as well. For example:

- In the FDD-A and FDD-C sub-panels, the operator can set and read the voltage and current applied by the high voltage boards to the PMTs.
- It can also monitor and control the status for each photomultiplier of the FDD-A and FDD-C sub-detectors.

4.3. CAEN boards temperature

Alarms were defined in such a way that the DCS operator can identify on the main panel if any of the sides of FDD detector has any type of problem:

- For example, the detector's green background of layer 1 of side C (Fig. 6) indicates that it is working correctly. However, the background changes to gray if there is a problem with that part of the detector.
- The operator can obtain more details of the problem by accessing the alarm panel. For example, the problem could be related to the temperature of the high voltage board for the FDD detector.

4.4. Voltage and current for PMTs

Another example of an alarm that was defined is the voltage level received by the PMTs connected to the FDD detector on side A and side C:

- The alarm is triggered either when the voltage level is above or below the set value.
- The same applies to the current level received by the PMTs.

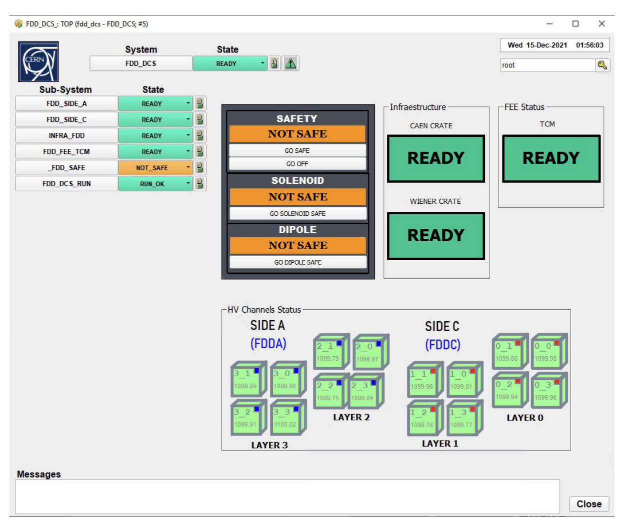

FIGURE 6. Main panel of FDD-DCS user interface.

5. Comments and outlook

The FDD detector was successfully constructed and installed in 2021. The FDD detector will increase the time resolution compared with AD detector used in Run-2 (2015-2018), and it will provide triggers at level zero for ALICE [12]. The software and hardware architecture already proposed will allow the release of a fully operative DCS for the FDD detector to comply with the new Online-Offline infrastructure requirements of the ALICE experiment. Finite State Machine testing is ongoing with WinCC-OA® software and high voltage boards. Finally, the Detector Control System development for FDD is progressing according to the plan and is expected to be ready for commissioning starting 2022.

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