

## LOW COST CONTRAST DETECTOR AND AREA EVALUATOR FOR SCANNING ELECTRON MICROSCOPY

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### ABSTRACT

Due to the importance of discriminating gray levels and measuring relative areas in a Scanning Electron Microscope, an electronic system, capable of doing this in 5 distinct levels, was designed. The logic involved in this system is similar to that of a multichannel analyser, but with two distinctive features; one is that it has the possibility of varying continuously the range of operation of one of the windows and the other feature is its low cost.

A detailed description of the circuits and their characteristics is given, along with design criteria. The system is sufficiently general, so as to be used in a great majority of SEMs, having marked advantages over conventional methods of image interpretation.

### 1. INTRODUCTION

The image in a scanning electron microscope (SEM), is obtained from the interaction of a thin electron beam, as it scans, with different points of a sample. Due to this interaction<sup>(1)</sup>, primary, secondary, absorbed and, in the case of thin samples, transmitted electrons are created. These electrons are collected by an electron-to-voltage transducer, and the voltages obtained are processed by a linear amplifier and fed to the Z axis of a cathode ray tube (CRT). Therefore the brightness on the CRT is proportional to the number of electrons collected, which in turn are proportional to the characteristics of the point observed.

The possibilities of processing the voltages from the transducer, before they enter the linear amplifier, are many and depend on the type of information that is required<sup>(2)</sup>. In this case, only the possibility of detecting or isolating one or more gray levels and comparing their area to the total area scanned, will be seen. The detection of a gray

level is equivalent to the detection of a voltage level, as was stated before; thus certain properties of the sample may be isolated.

The processing of the voltage from the transducer requires the use of an electronic logic system, as in the multichannel analyser, called window, with the following characteristics:

$$V_{\text{out}} = \begin{cases} 1 & \text{if } V_{\text{in}} \in [V_0, V_1] \\ 0 & \text{if } V_{\text{in}} \notin [V_0, V_1] \end{cases} \quad (1)$$

Where  $V_{\text{in}}$  is the signal from the transducer, 1 and 0 are logic levels,  $V_{\text{out}}$  is the output voltage (which will now be applied to the linear amplifier) and  $V_0$  to  $V_1$  define the voltage level and interval that is to be isolated. A necessary requirement is that:

$$V_0 < V_1 \quad (2)$$

To enhance the efficiency of this technic and for a more rapid interpretation of the new image, a series of windows with a minimum overlap and that cover the range of voltages produced by the transducer, are used (fig. 1). In this case five windows ( $W_i$ ,  $i = 1$  to 5) were set, so that

$$V_0 \text{ of } W_{i+1} = V_1 \text{ of } W_i \quad (3)$$

with  $V_0$  of  $W_1$  equal to the black level and  $V_1$  of  $W_5$  equal to the white level of the CRT. The range of the five windows has the same width and two or more windows may be used simultaneously if need be.

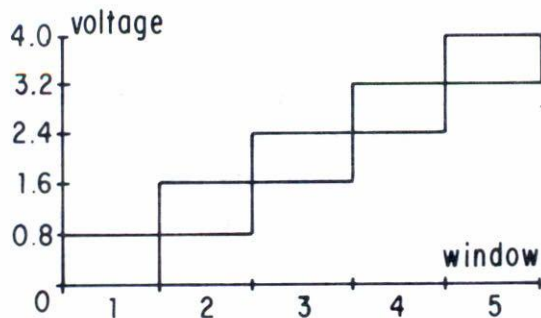


Fig. 1. Voltage range covered by  $W_1$  to  $W_5$ .

The importance of this system, is not only the possibility of detecting gray levels, but also the evaluation of the area covered by a gray level ( $A_G$ ) as a function of the total area scanned ( $A_T$ ). This is accomplished by measuring the time that the window is open ( $T_G$ ) and comparing with the time used in one scan of the sample ( $T_T$ ). The following equation is immediate:

$$\frac{T_G}{T_T} = \frac{A_G}{A_T} \quad (4)$$

So as to have more flexibility, instead of only using the fixed value windows, a sixth window ( $W_6$ ) is implemented with  $V_0$  and  $V_1$  variable, for area evaluation. The only requirement is that equation (1) be observed.

## 2. FLOW AND BLOCK DIAGRAMS

To give a general idea of the system proposed, flow and block diagrams will be analyzed first.

### 2.1 Flow diagram of the function selector

The voltage signal from the transducer is connected to a five pole, three position commutator switch (sw.1), Fig. 2 called function selector. With the first pole (sw.1.A) the first position sets the signal directly to the linear amplifier of the SEM; the second position connects the signal to the five fixed windows, the window or windows to be used are selected by the switches sw.2,3,4,5 and 6; the last position of sw.1 connects the signal to the variable window,  $W_6$ . The second pole (sw.1.B) connects the appropriate output to the linear amplifier of the CRT, the third pole (sw.1.C) and the fourth pole (sw.1.D) connect the bias voltages accordingly, and (sw.1.E) connects the area counter to the window or windows to be used.

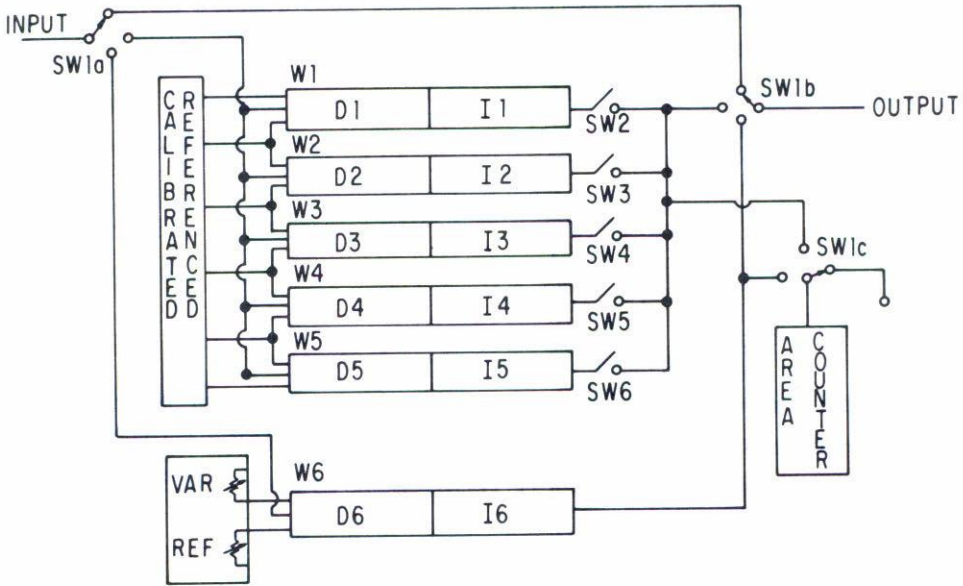


Fig. 2. Block diagram of the entire system: Windows, composed of voltage references, level detectors (D) and inverters (I).

## 2.2 Block diagram

The five fixed-level windows, figure 2 are formed by two blocks, the level detector and the logic inverter. The voltage references for the windows are chosen and calibrated according to the SEM used. The sixth window has the same configuration of the others but the voltage references are variable, as said before and condition 2 is kept.

The area counter figure 3, is formed by: a) a high frequency (1 MHz) pulse generator, b) a complex gate and c) two identical sets of frequency dividers, pulse counters and displays.

The pulses of the generator pass onto one of the sections of frequency dividers, counters and displays by means of the complex gate during the first scan, after resetting the gate. Pulses go to the other frequency divider, counter and display only when the sixth window has a logic 1 at its output, during the scan. After the first scan, once the



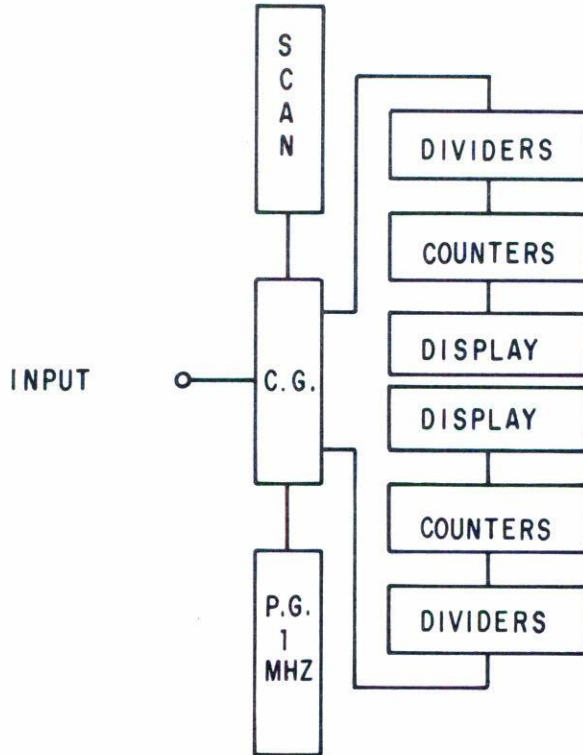


Fig. 3. Area counter, composed of a complex gate (CG), a pulse generator (PG), frequency dividers, counters, displays and scan synchronization.

complex gate is reset, there is no possibility of accumulating more counts; if the gate is reset, all information is lost and everything is ready for a new count.

### 3. CIRCUITS AND DESIGN CRITERIA

A detailed description of the different blocks of the system and the criteria for the selection of these components is now given.

#### 3.1 Level detector

This is the fundamental piece of the system and is basically formed with a  $\mu 711c$  (CI.1) type microcircuit figure 4a. The  $\mu 711c$  was selected for its fast response time<sup>(3)</sup> (0.4  $\mu\text{sec}$ ) because the window must be able to distinguish a change in voltage occurring in less than 5  $\mu\text{sec}$ .

This is the time separation between adjacent points on the CRT at a 5 sec/frame and  $10^6$  points/scan, which is the minimum time for taking fair photographs. The condensers C.2 and 3 eliminate parasitic high frequencies, inherent to a SEM, that would affect the 711. The voltage signal from the transducer is applied via R.2 and the reference voltage  $V_0$  and  $V_1$  via R.3 and R.1 respectively. Condensers C.1, 2, 4 and 5 eliminate instabilities that appear in the 711s', when the signal voltage coincides with any of reference voltages.

The output logic of the 711 is such that for  $V_{in} \in [V_0, V_1]$  the output is a logic "zero" and for  $V_{in} \notin [V_0, V_1]$  it is a logic "one". So as to fulfill the specifications of (1), a (logic) inverter is placed at the output of the  $\mu$ A711.

### 3.2 The inverter

This section, figure 4b, has a transistor T.1 in a common emitter

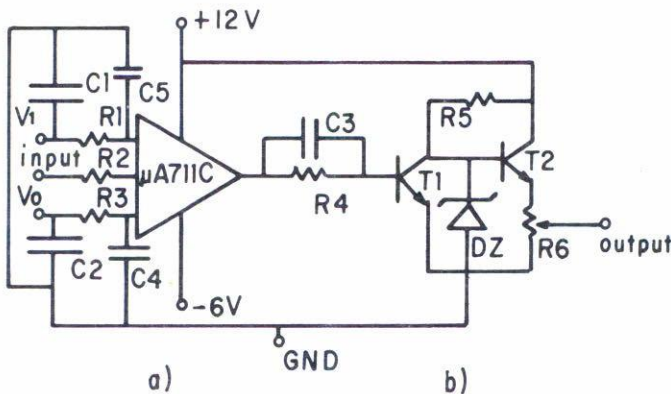


Fig. 4. Window's components: a) level detector and b) logic inverter.

configuration and is connected to the  $\mu$ A711 by means of R.4 and C.1. From the collector of T.1, the inverted voltage signal passes to T.2, which provides lower output impedance than T.1. The maximum collector voltage of T.1 is limited by the zener diode Dz.1 and the output voltage is taken from the center tap of the potentiometer R.6. The output is adjusted with R.6, so that the logic "one" provides a white tone on the CRT; the logic "zero" provides a black tone independently of the setting of R.6.

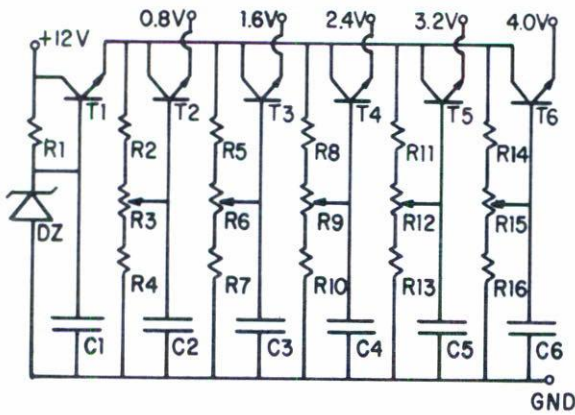
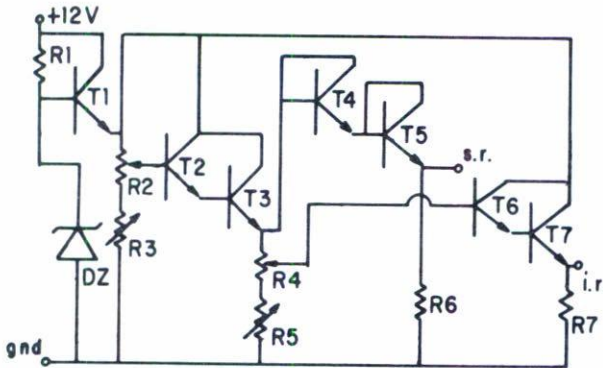


Fig. 5.

a. Reference voltages for fixed-level windows.



b. Variable reference voltages for  $W_6$ , the outputs being the superior reference (sr) and the inferior reference (ir).

### 3.3 References voltages

This block, fig. 5a, provides the references voltages for the five fixed-value windows according to 2 and 3. The aperture ( $V_1 - V_0$ ) is the same for each window and for the SEM S-600, the reference voltages are 0v, 0.8v, 1.6v, 2.4v, 3.2v and 4v. These voltages are set by the potentiometers R.3, 6, 9, 12 and 15, at the emitters of the transistors T.2 to 6 respectively; the emitters being connected to the  $\mu 711$ s' reference voltage inputs. Zener diode Dz.1 and transistor T.1 maintain a constant bias voltage for the circuit and the range of the reference voltages (0v to 4v) may be modified by changing Dz.1.

### 3.4 Variable references

The variable references, figure 5b, are controlled by the setting of two ten-turn potentiometers, R.2 and R.4. The constant reference voltage obtained from the emitter of T.1, due to the zener diode Dz.1, is connected to R.2; according to the setting of R.2, transistors T.2, 3, 4 and 5 will supply the reference voltage  $V_1$ . Transistor T.4 and 5 are needed to produce voltage drops approximately equal to those of T.6 and 7. Due to this configuration, the maximum voltage ( $V_o$ ) that R.4 can set by means of T.6 and 7 is the voltage  $V_1$ , this protects the window of unallowed states in accordance to eq. 2. The trim potentiometers R.3 and 5 are used to compensate the base-emitter voltage drops of the transistors and R.6 and 7 are the output resistance that the circuit presents.

### 3.5 Area counter

According to equation 4, the relative measurement of area ( $A_G/A_T$ ), can be determined by the time intervals  $T_G$  and  $T_T$ . One method of doing this, is by counting the numbers of periodic pulses during the said time intervals.

#### 3.5.1 Pulse generator

The precision with which the counts are to be made, depends on a) the stability of the pulse generator and b) the number of pulses per unit time (frequency).

A frequency generator of 1MHz was chosen so that at a scan speed of 5 sec/frame there will be at least four pulses per point duration on the CRT. To guarantee the stability of the generator, a quartz crystal was used in an astable multivibrator circuit, formed with two NAND gates<sup>(4)</sup>, figure 6, and two gates were used as inverters to square the wave generated. Condenser C.1 trims the oscillation by  $\pm 10$  cycles and the frequency obtained was  $1,000,000 \pm 1$  Hz, during a two hour measurement. Scanning speeds of 2000 sec/frame or lower may be used with this system because of the high and long term stability of the oscillator.



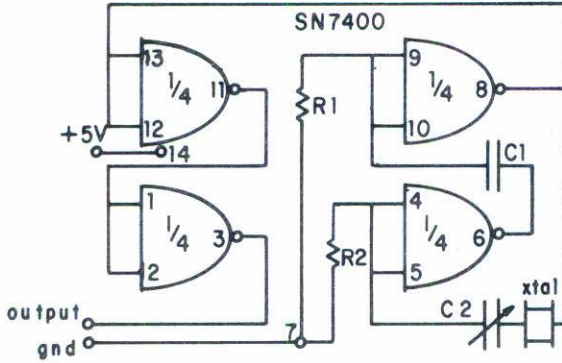


Fig. 6. Pulse generator (1MHz).

### SCAN SINCORIZATION

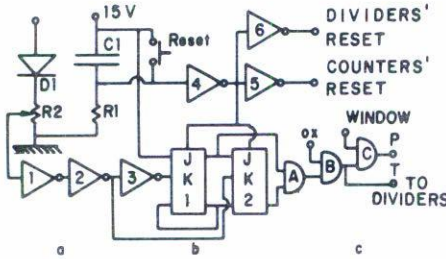


Fig. 7. Complex gate and resetting logic. Output (G) gives the gray level scan time and output (T) the total.

### 3.5.2 Complex gate

The pulses to be counted, are selected by means of the complex gate (fig. 7). This is done by with the aid of three AND gates<sup>(4)</sup> (A, B and C) that permit the pulses from the generator to pass onto the frequency dividers, counters and displays (which are seen in section 3.5.3), according to the information provides by the reset control, the scan synchronization signal and the state of the variable window. With the exception of the inverter of section 3.2, all other logic component are TTL.

In order to have a count during only one scan, the JK-flip-flops are in a configuration, such that: after resetting them there is a (logic) ZERO at the Q output of flip-flop FF.1, a ONE at  $\bar{Q}$  of FF.2; therefore gates A, B and C have ZEROES at their outputs. When the

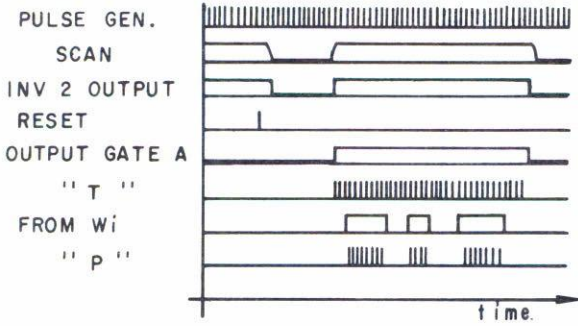


Fig. 8. Schematic of signals at different points of the complex gate, simulating a measurement of the partial area selected by the window.

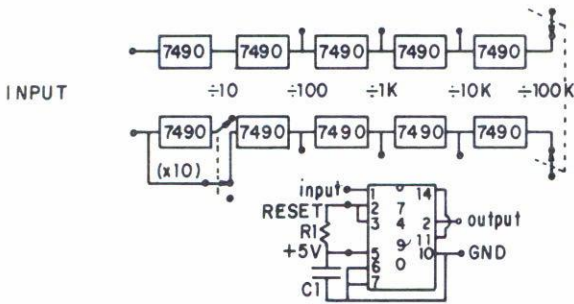


Fig. 9. Frequency dividers and  $\times 10$  multiplier switch with sw. 2 for  $T_G$ .

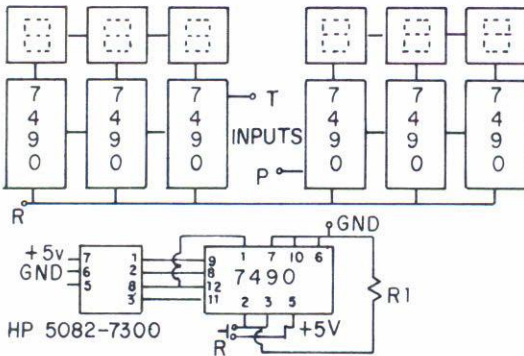


Fig. 10. Counters and Displays.

scan pulse appears (ZERO to ONE transition) at the input of inverter 1, FF.1 is clocked by the negative going transition (ONE to ZERO) at the output of inverter 3, inverters 1 and 2 are only used to square the pulse. Due to the fact, that only negative going transitions clock these flip-flops, FF.2 remains unchanged. Therefore the scan pulse, when it appeared, changed the Q output of FF.1 to a ONE, and this in turn, sets a ONE at the output of gate A. Gate B has a ONE at one input, hence the pulses of the frequency generator at the other input, appear at the output and are passed onto one set of frequency dividers, counters and displays. The pulses at the output of gate B are also present at one input of gate C and only appear at gate C's output when its other input is a ONE; this only happens when the voltages from the transducer are in the range set by variable window. When the scan pulse ends, FF.2 changes its  $\bar{Q}$  output to a ZERO, therefore the output of gate A becomes a ZERO and as explained before, no more pulses may pass through gates B and C. The connection between  $\bar{Q}$  and K ties down FF.1 after the first clock pulse and therefore flip-flop 2 becomes tied down after its first clock pulse. Having the logic tied to one state, after resetting it and having the first scan pulse, eliminates the possibility of having another count superimposed on the first one. Figure 8 gives a more clear idea of the behavior of the complex gate by showing what occurs at different points and times.

### 3.5.3 Frequency dividers, counters and displays

This section consists of two identical sets of: 5 frequency dividers (type 7490), fig. 9, 3 counters<sup>(4)</sup> (type 7490) and 3 displays<sup>(5)</sup> (type HP-5082-7300) fig. 10. The number of pulses that enter a divider is divided by ten and the number of dividers used is set by switch sw.1 for both sets. According to the scan period, sw.1 is set so as to have no more than  $10^3$  pulses out of the last divider for the total area count. Hence one display will give the total area ( $A_T$ ) in three digits and the partial area ( $A_G$ ) will be equal or less according to the variable window limits. If  $A_G$  is too small, its value may be displaced on the display by an order of magnitude, by means of switch sw.2, which overrides the first divider of the set where gate C is connected.

The counters, simply accumulate the number of pulses from the last divider used and display this number through the digital readout display. In case that four digits are required for  $A_T$ , the following procedure is used: a) Scan and read  $A_T$  with three digits and read  $A_G$ , b) Lower by one the number of dividers used with sw.1, c) Scan and read the new numbers and d) Place the most significant number of the first readings in front of the second readings. The time precision with which a SEM works is not comparable to that of the frequency generator, therefore only the first significant number of the first reading has any bearing on the second reading.

### 3.6 Power supplies

The power supplies were designed with a 0.1% ripple factor and a high rejection ratio to line variations.

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