Phosphorus ion implantation gettering effects in MOS structures

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ABSTRACT. The influence of some variables of phosphorus ion implantation gettering on the gettering efficiency in MOS capacitors was investigated by the C-t measurement technique. The Si wafers were gettered by a 120 keV backside P ion implantation, into bare silicon and into silicon covered by a screen oxide 600-1200 Å thick, with subsequent annealing at 900°C for 30-150 min in N_2. The generation lifetime was found to show maximum value after 120 min anneal. A marked tendency in the behavior of generation lifetime, when P was implanted into bare silicon and when it was implanted into silicon covered by an oxide, was not found. In both cases, the generation lifetime increases with the increase of oxide thickness.

RESUMEN. La influencia de los parámetros de la implantación iónica de fósforo, en los procesos estabilizadores (gettering), sobre la eficiencia de"gettering" fue investigada usando la técnica C-t en capacitores MOS. Las obleas fueron estabilizadas por medio de implantación iónica de Fósforo en el silicio descubierto y cubierto con una pantalla de óxido de 600–1200 Å con un reconocido subsecuente a 900°C por 30–150 min en N_2. El tiempo de vida de generación muestra un máximo despues de 120 minutos de recocído. No se encuentra ninguna tendencia marcada cuando se implanta a través de óxido o sin él, pero en ambos casos el tiempo de vida de generación aumentó con el aumento del grosor de óxido.

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1. INTRODUCTION

Ion implantation gettering is one of the means of reducing and/or eliminating metallic impurities and other kinds of crystalline defects in a wafer or, at least, in its device-active region. Different ions (Ar, Kr, Ne, Xe, O, P, B, Si) have been used to create ion damage [1-5]. Seidel *et al.* [1] have ranked the gettering efficiency of the damage produced

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by different ions in the order Ar $\geq$ O > P > Si > As > B. They have found that the gettering efficiency of these ions is less than that of phosphorus diffusion at 1000°C.

Gregor and Stinebaugh [6] have shown that a phosphorus implantation combined with a segregation anneal, has almost the same gettering effectiveness as phosphorus diffusion at 1000°C. They found that gettering efficiency appears most effective at 700-800°C and decreases with the increase of temperature, depending on the final high temperature treatment.

Geipel and Tice [7] reported that the gettering efficiency of 170 keV Ar implantation performed through a 500 Å thick oxide layer, can be equal or greater than that performed in bare silicon, depending on the dose. In general, for equal gettering efficiency, lower doses are required for implantation through an oxide layer. This fact was explained assuming that knock-on oxygen atoms produce a significant portion of the ion-implant damage and this way the gettering efficiency is increased.

Beyer and Yeh [8], did not find a significant relaxation time difference between Ar implantation gettering performed, with and without an oxide layer using a dose of 10^{16} atoms/cm^2 and a 900°C segregation annealing. However, they have found that for annealing at 1000 and 1100°C, the relaxation time is longer for samples implanted through an oxide layer, in spite of the fact that the projected range in SiO_2, 483 Å at 60 keV, is smaller that the oxide thickness (600 Å). Moreover, they found that when the oxide thickness increases, the relaxation time increases.

They didn't explain the segregation temperature dependence of gettering efficiency. The increased gettering efficiency for implantation through an oxide layer was also explained assuming that the knock-on oxygen atoms produce a significant portion of the ion-implant damage.

Gong and Schroder [9], which performed a similar experiment, found a small lifetime difference between the Ar implants into bare and into oxide covered silicon. In the last case, the lifetime was a little higher. They attributed this to the impurity screening effect of the oxide. If there is no screening oxide present, they assume metallic atoms from the furnace diffuse into the silicon.

There are a number of gettering models that have been proposed, but none of these models explains all observed effects under a given set of gettering conditions.

According to the enhanced metal solubility model, the solubility of any element is altered by the presence of other charged impurities if the concentration of these impurities effects the Fermi level [10-13].

There are experimental results which contradict this model, demonstrating that raising the Fermi level by increasing the concentration, does not enhance gettering effectiveness [1,14,15].

Extrinsic gettering techniques such as solute diffusion, mechanical damage, ion implantation, laser damage, non metal film deposition and intrinsic gettering have been explained by the extended defect model. The extended defects, especially dislocations, interact with the impurities [16] and act as sinks for metallic impurities, thus providing a gettering effect. The elastic interaction between point defects and dislocations, arising from the difference in size between solute and solvent atoms, is the dominant one in this model.

There are experimental evidences that dislocations and/or oxidation stacking faults (OSF) are not a prerequisite for efficient gettering [14,15,17,18]. On the other hand, there are many experimental evidences that metallic impurities such as Cu, Ni, Fe, Zn and Sn do precipitate preferentially towards defects; this is why the extended defect model cannot be rejected.

Ourmazd and Schröder [19] have suggested that supersaturation of Si self-interstitials may be responsible for the low-temperature phosphorus diffusion gettering when no dislocations are generated. Phosphorus diffusion causes SiP particle formation which, due to a volume expansion, leads to a large emission of silicon interstitials. When Ni is present, the volume expansion relaxes due to $NiSi_2$ growth, and consequently, the interstitial emission is reduced at the Si/PSG (Phosphosilicate glass (PSG)) interface, thus resulting in Ni gettering.

Phosphorus gettering of Pt in silicon was also explained by Falster [20] with a model based on Si self-interstitials. According to this model, self-interstitials kick out low-mobility, high-solubility substitutional Pt into high-mobility, low-solubility interstitial sites. Then the interstitial Pt diffuses to the sinks at the wafer surface. It is well known that oxidation (at least for short oxidation times) and oxynitridation supersaturate silicon self-interstitials.

The gettering of Au in silicon can also be explained by this model.

However, there are many experimental observations which can not be explained by the self-interstitial model [14,15,21,22]. Some authors [21,22] explain this assuming that oxidation generates less Si interstitials than does, for example, P diffusion, or that Si interstitials are annihilated at trap centers (oxygen precipitates).

Baldi *et al.* [23] proposed the segregation model, which belongs to the enhanced metal-solubility family. The segregation model is developed thermodynamically and metal solubilities in undoped as well as in doped regions are taken into account. This means that a segregation coefficient of the metals, between the gettered site and the silicon matrix, exists. According to this model, the segregation coefficient, and thus the gettering efficiency, increases as the gettering temperature decreases. This is not always true [8]. On the other hand, there are experimental results which demonstrate the gettering efficiency of the damaged layers.

Finally, Kang and Schroder [15] tried to generalize the segregation model including in it gettering due to extended defects.

As can be seen, in spite of the great number of papers published on gettering, there are many contradictions and the exact mechanisms by which gettering comes about have not been well established yet.

Ion implantation is a widely used process step in Integrated Circuit (IC) technology. VLSI MOSIC's need low temperature process steps and the ion implantation gettering, with low temperature anneal, can be used in this case as a standard process step.

Ion implantation gettering basically consists of two process steps; creation of an ion-damaged layer followed by gettering at elevated temperature. From the physical point of view, the gettering process involves three steps which are carried out during high temperature fabrication process treatments. The first step is the release of defects (metallic impurities, for example) from their associated forms, the second step is diffusion of defects to the gettering region, and the third is the capture of defects at the gettering sites. Finally,

TABLE I. Parameters of the principal process steps.

Wafer	Oxidation T (°C)	Oxidation t (min)	Oxide Thickness Å	Annealing, N_2 1000°C t (min)	P ion implantation Energy (KeV)	P ion implantation Dose (at/cm^2)	Annealing, N_2 T (°C)	Annealing, N_2 t (min)
G_1	1000	90	800	30	120	10^{16}	—	—
G_2	"	"	800	"	"	"	900	30
G_3	"	"	800	"	"	"	"	60
G_4	"	"	800	"	"	"	"	90
G_5	"	"	800	"	"	"	"	120
G_6	"	"	800	"	"	"	"	150
G_9	"	70	600	"	"	"	"	80
G_{10}	"	110	1000	"	"	"	"	80
G_{11}	"	30	1200	"	"	"	"	80

once that defects are captured at the gettering sites, they can be released again at high temperatures. When released, they can reach the active region of the wafer, depending on annealing time and temperature.

There are very few papers devoted to P ion implantation gettering but, as it was shown [6], it can be as effective as P diffusion.

The purpose of this work is to investigate the influence of some variables of phosphorus ion implantation gettering, on the gettering efficiency in MOS structures, as well as to clarify some model concepts. The gettering efficiency of phosphorus implantation through a masking oxide and into bare silicon was also investigated.

2. SAMPLE PREPARATION AND MEASUREMENTS

N-type (100) 2.5-5 ohm-cm silicon wafers were used in this experiment. The wafers were cleaned ultrasonically and RCA washed after that. They were oxidized at T=1000°C in dry O_2 + 2% TCA (C_2 H_3 Cl_3) ambient, then annealed in N_2 at T=1000°C for 30 min. Different oxide thicknesses were obtained by varying oxidation time. Details of the process steps are presented in Table I. As shown in Fig. 1, the back oxide on one half of all wafers was removed. Backside phosphorus ion implantation with a dose of 10^{16} atoms/cm^2 and 120 keV energy was performed. After that, 100 Å of SiO_2 were removed in order to prevent metallic contamination. The ion implanted damage was annealed at T=900°C in N_2 for different times (see Table I).

Aluminum dots, for MOS structures, were deposited through a metal mask on the top oxide. The backside oxide was striped and aluminum was deposited to make the backside contact. All wafers were sintered in a N_2/H_2 ambient at 425°C for 30 min.

MOS C-t measurements were performed at 1 MHz using a PAR model 410 capacitance meter to determine the generation lifetime.

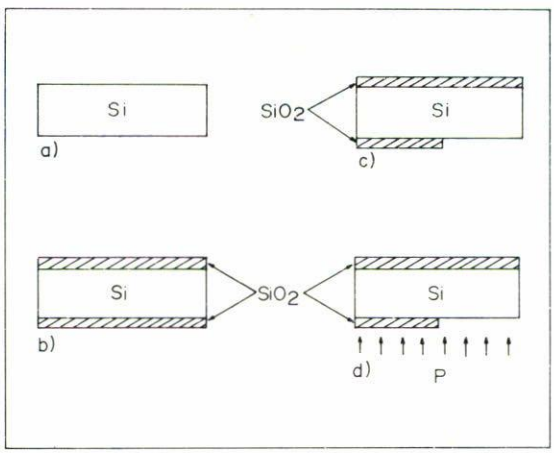

FIGURE 1. Process sequence: (a) Si wafer, (b) both sides wafer oxidation, (c) etching half of the backside oxide, and (d) backside P ion implantation.

3. EXPERIMENTAL RESULTS AND DISCUSSION

The first experiment was designed to investigate the influence of post gettering annealing (segregation annealing) time, on the gettering efficiency, for oxide-covered and bare silicon surfaces. According to the concept of the gettering process, impurities must be released from their original sites, diffuse to the gettering region, and be captured, at the gettering sites. The segregation model states that, by decreasing temperature, the segregation coefficient, and thus the gettering efficiency will increase. However, one of the three gettering steps (release, diffusion, capture) will be the rate-limiting step for gettering. For instance, decreasing temperature, the diffusivity of impurities will be reduced and for short annealing times, the distance between the impurity site and the gettering site will be longer than $2(D_1 t)^{1/2}$, the impurity diffusion length, were D_1 and t are the impurity diffusion coefficient and its diffusion time, respectively.

Generation lifetime as a function of the annealing time, for implantation into bare silicon and through a screen oxide is shown in Figs. 2 and 3, respectively. Each point on the curves represents the mean value of generation lifetime measured in 20 MOS capacitors. The mean sample standard deviation was 3.2×10^{-5} and 2.5×10^{-5} for the data in Figs. 2 and 3, respectively.

The curves indicate a gettering efficiency which increases, rapidly, with annealing time to 30 min between 30 and 90 min, there is a plateau and after 120 min the efficiency increases again. For annealing times greater than 120 min, the gettering efficiency decreases.

On the basis of these experimental results, it could be assumed that two types of impurity defects are responsible for this behavior of τ_g. The first one is a fast diffusing impurity which is gettered at around 30 min. The second, is a slower one, diffusing from the original impurity site to the gettering region in about 120 min.

Two reasons can be responsible for the generation lifetime decrease after 150 min. First, one would expect that during annealing, metallic atoms from the furnace diffuse into the silicon bulk. Second, after 150 min annealing, it could be supposed that the

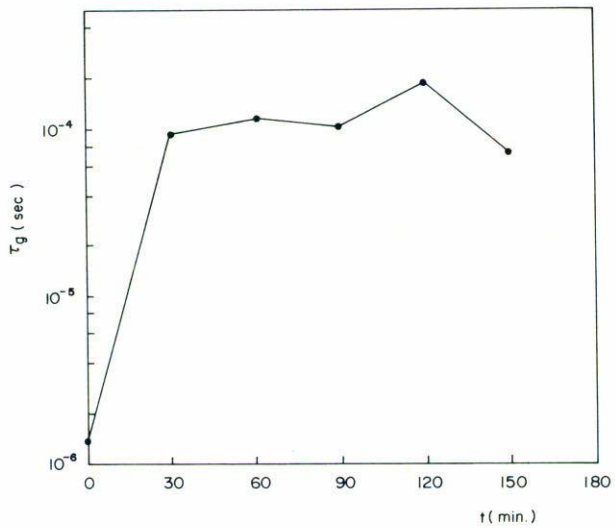

FIGURE 2. Generation lifetime as a function of annealing time for P implantation into bare silicon.

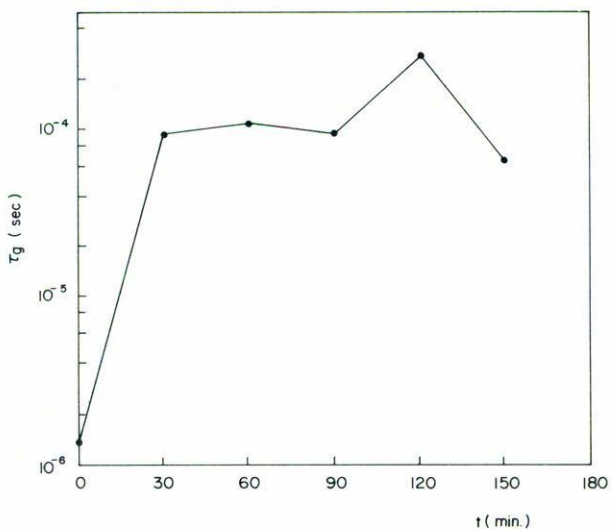

FIGURE 3. Generation lifetime as a function of annealing time for P implantation into silicon covered with oxide.

damage created by the implantation starts to be annealed (repaired). This means that the impurities captured at the gettering sites start to be released.

In Table II the ratio of $\tau_g(b)$, corresponding to the half of the wafer covered with a screen oxide, to $\tau_g(a)$ corresponding to the half of the wafer without oxide, is presented for all wafers. This ratio for wafer G_6, annealed 150 min, is 0.91. If only metallic contamination from the furnace was responsible for the decrease of the generation lifetime after 150 min anneal, this ratio should be grater than 1.

TABLE II. Ratio for τ_g (b) to τ_g (a) for the corresponding segregation time at 900°C in N_2.

Wafer	G_1	G_2	G_3	G_4	G_5	G_6	G_9	G_{10}	G_{11}
t_{an} (min)	0	30	60	90	120	150	80	80	80
$\frac{\tau_g(b)}{\tau_g(a)}$	—	1.00	3.64	0.92	1.44	0.91	0.92	0.64	1.20

It could be assumed that the main reason for deteriorated gettering efficiency after 150 min anneal, is the annealing of the ion implantation damage, with the subsequent release of impurities from their gettering sites. In our previous experiment [24] P ion implantation gettering was done with a 2×10^{15} atoms/cm^2 dose and with the same energy (120 keV), but the annealing was performed at 1000°C. It was shown, in that case, that gettering efficiency decreases after 60 min anneal. Comparing the results of both experiments, it can be concluded that the degree of ion damage increases with implanted dose (but too high a dose can cause dislocations to overlap and relieve strain, reducing their ability to getter) and is more permanent when the annealing is carried out at lower temperatures. However, the influence of metallic impurities diffusing from the furnace into silicon during annealing, can not be excluded totally. It was also shown [24] that generation lifetime in MOS structures without gettering decreases after 90 min anneal. It can be supposed that both mechanisms compete, and for given experimental conditions, one will dominate.

The purpose of the second experiment was to investigate the role of the screening oxide in ion implantation gettering. Generation lifetime as a function of the screening oxide thickness is shown in Fig. 4. It must be mentioned here that the gate oxide was grown together with the back screen oxide, and thus has the same thickness. The generation lifetime in the halves of the wafers without a screening oxide is also presented in Fig. 4. The projected range of 120 keV P ions is 1215 Å in SiO_2 [25].

Clearly, the major portion of the implanted P remains in the silicon for a 600 Å oxide thickness. With the increase of oxide thickness, the phosphorus ion concentration in the wafer decreases, and for a 1200 Å oxide thickness almost half of the implanted P remains in the oxide. Nevertheless, generation lifetime or gettering efficiency increases as the oxide thickness increases, as can be seen from Fig. 4.

As it was mentioned in part I, Gong and Schroder [9] ascribe an impurity screening effect to the back oxide. Blyer and Yeh [8] assume knock-on oxygen atoms increase ion-implant damage and they increase gettering efficiency. However, as can be seen from Fig. 4, generation lifetime in both halves of the wafers increased as the oxide thickness (or oxidation time) increased. This means that there must exist another mechanism which plays an important role.

The increase of generation lifetime with the increase of oxidation time (or oxide thickness) has been already reported [26].

It is well established that oxidation causes silicon self-interstitials to flow into the crystal, which leads to nucleation and growth of OSF, which are the main reason for the decrease of generation lifetime. However, it has also been shown that for long oxidation times, and in the presence of chlorine-bearing species (TCA in our case), the OSF's

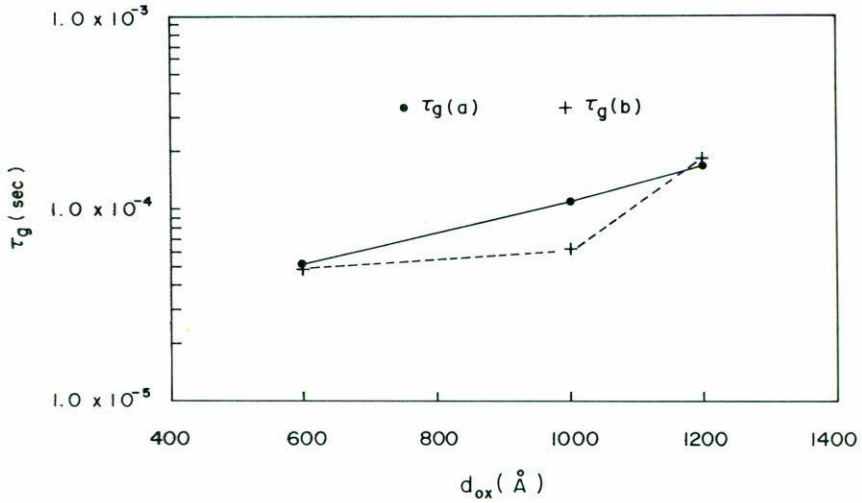

FIGURE 4. Generation lifetime as a function of oxide thickness: for P implantation into bare silicon (·) and for implantation into silicon covered with oxide (+).

Shrink [26-28]. In a chlorinated ambient Si atoms are removed from lattice sites by chlorine molecules, and vacancies are thus generated. On the other hand, for long oxidation times (thick oxide) the Si-SiO_2 interface acts as a less efficient interstitials source [27]. It could also be thought that another source of vacancies exists.

4. CONCLUSIONS

We have investigated the influence of segregation anneal on gettering efficiency of P ion implantation through bare and oxide covered silicon by the MOS C-t technique, measuring generation lifetime. It was found that maximum gettering efficiency at 900°C was obtained before 120 min anneal. After that time, generation lifetime decreases and it was attributed to damage produced by ion implantation starts to be annealed. However, metallic contamination from the furnace cannot be excluded.

The increase of generation lifetime with the increase of oxide thickness was supposed to be due mainly to shrinkage of the OSF's.

On the basis of our experiments, the following main conclusions, concerning the existing gettering models, can be made:

1. The process of gettering cannot be explained with only one of the existing models.

2. The mechanisms included in the segregation and enhanced defect models, play a dominant role in the process of gettering.

3. The segregation annealing time, which has not received sufficient attention in the literature, plays an important role in the process of gettering. The processes of release and diffusion of metallic impurities to the gettering region depend on it.

The anneal of ion implantation damage, the subsequent release of captured defects and their diffusion back to the device active region, also depend on annealing time. On the other hand, if the metallic impurities from the furnace influence generation lifetime, the process will also be time dependent.

4. In spite of the fact that the role of the back side oxide during implantation gettering is still not clear, it is evident that oxidation conditions (ambient, temperature, and oxidation time) play an important role in the final gettering efficiency.

Isothermal post-gettering segregation annealing can be used to investigate the nature of the impurities responsible for the behavior of generation lifetime. In the following paper we will try to identify the impurities responsible for the degrading of generation lifetime.

A lot more experimental and theoretical work must be done to clarify the different mechanisms taking part in the process of gettering.

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