

Investigation of the anisotropic etching process used for semiconductor pressure sensors fabrication

P. PEYKOV*, S. ALCÁNTARA

*Departamento de Semiconductores, Instituto de Ciencias
Universidad Autónoma de Puebla
Apartado postal 1651, 72000 Puebla, Pue., México*

M. ACEVES, M. LINARES

*Instituto Nacional de Astrofísica, Óptica y Electrónica
Apartado postal 51 y 216, 72000 Puebla, Pue., México*

AND

C. RAMÍREZ, R. GALEAZZI

*Departamento de Semiconductores, Instituto de Ciencias
Universidad Autónoma de Puebla
Apartado postal 1651, 72000 Puebla, Pue., México*

Recibido el 30 de septiembre de 1991; aceptado el 22 de septiembre de 1992

ABSTRACT. The anisotropic etching of (100) oriented silicon wafers with 34% KOH in the temperature range 35–60°C was investigated. The etch rate of silicon in (100) and (111) crystallographic direction as well as the etch rate of thermally grown SiO₂ is determined. It was found that the angle between the (111) walls of the etched grooves and the surface (100) plane can be different from the theoretically calculated value 57.74°.

RESUMEN. Se investigó el grabado anisótropo de obleas de silicio con 34% de KOH en orientación (100), a temperaturas en el intervalo de 35–60°C. Se determinó la razón de grabado para las orientaciones cristalográficas (100) y (111). También se determina la razón de grabado del SiO₂ que creció mediante un proceso térmico. Se encontró que el ángulo entre las paredes (111) de las ranuras grabadas y la superficie (100) puede ser diferente del valor calculado teóricamente de 57.74°.

PACS: 43.88.Gy

1. INTRODUCTION

Wet chemical etching has been used in silicon semiconductor processing since the early 1950's. An isotropic etcher etches in all crystallographic directions at the same rate. These are used for etching and chemical polishing of silicon wafers [1-3]. In the more recent past, anisotropic or orientation-dependent etchers have been used [4-6]. The anisotropic chemical etching of a single crystal silicon wafer, resulting from the different etch rates of its crystallographic planes, has been used to fabricate a variety of active and passive three

*On leave from University of Sofía, Sofía, Bulgaria.

dimensional device structures such as X-ray masks [6-8], optical wave guides [9], high-resolution patterns [10], nozzles [11], micro tools [12], diodes [13], bipolar and MOSFET circuits [14,15], electromechanical [16] and micromechanical [17] devices, and pressure sensors [18].

The anisotropic etching of Si is influenced by the following main factors: (i) the crystallographic perfection of the substrate; (ii) the geometry and the orientation of the surface pattern, which is delineated by the masking film on the substrate surface; and (iii) the experimental conditions.

Peterson [19] has reviewed and summarized the data of common wet silicon etch experiments, such as etch type and concentration, wafer crystallographic orientation, masking film and working temperature.

A KOH-H₂O mixture offers many advantages such as process simplicity and etch anisotropy. For the case of a KOH etcher the working temperature is normally high ($\sim 85^\circ\text{C}$) and the masking film is Si₃N₄. Some experiments performed with 44% KOH-H₂O and SiO₂ as a masking film of (110) oriented Si wafers are also reported [20]. However, this etcher exhibit a different preferential etching behavior which has not been adequately explained yet [19].

For many years it was not known why the etch rate and surface quality, on the (100) Si surface, are so variable when using a KOH-H₂O mixture. Furthermore no definitive suggestions were made to explain the difference in the etch rates of (100), (110) and (111) Si surfaces, other than general observation regarding the dangling bond densities for the different crystallographic orientations. These are 1.36×10^{15} , 0.96×10^{15} and $0.78 \times 10^{15} \text{ cm}^{-2}$ on the (100), (110), (111) surfaces, respectively.

Kendall [20] proposed that the slow etch rate of (111) Si in KOH-H₂O is due to the simultaneous oxidation and dissolution processes. According to this model, the (111) surface was thought to develop an oxide film in the solution that blocks etching. The subsequent oxide dissolution was then the limiting step in the Si etching process. The other crystal planes were thought to oxidize more slowly, and not to have chance to fully passivate, so they dissolved continuously. This would mean that at lower temperatures the etch rate of the (111) surface would be as low as that for SiO₂ but it is not true. On the other hand, it has been shown that the (111) surface is not the plane that oxidizes most rapidly [23].

According to a recent model [24], the slow etch rate of the (111) surface is due to the fact that it is blocked from the etching process by inactive complexes. It has been shown that the (111) surface is strongly passivated against etching in a KOH solution by attachment of OH:3H₂O⁻ ion complexes to each surface atom. Only the free water molecules can attack the {111} surface, with no OH⁻ ion involvement. As the molarity of the solution increases, the OH⁻ concentration increases, while hydration effects reduce the free H₂O concentration available for dissolution. These two effects produce a peak in the etch rate which is sensitive to the mean hydration number.

The purpose of this work is to investigate the anisotropic etching process for fabrication of thin silicon diaphragms under specific experimental conditions: (100) oriented n-type Si, 34% KOH etcher, SiO₂ as a masking film and working temperature in the range 35°-60°C. This work is a part of the project for development of silicon pressure sensors.

2. EXPERIMENTAL CONDITIONS

CZ grown, n-type Si wafers, 2-5 ohm-cm, (100) oriented were used in this study. A masking film of thermally grown SiO_2 was used. The wafers were oxidized in water vapor at $T = 1200^\circ\text{C}$ to obtain an 8000 Å oxide layer. Using a conventional photolithographic technique square windows with dimensions $465 \times 465 \mu\text{m}^2$ were opened in the top oxide.

The anisotropic etching was performed by the use of 34% potassium hydroxide (mixture of KOH and deionize water) solution.

After the removal of the native SiO_2 in the windows the wafers were put in the pyrex vessel containing the etch solution at the desired temperature, which was kept constant by a Blue M constant temperature bath, within $\pm 1^\circ\text{C}$ by means of a proportional electronic temperature control unit. The experiments were performed at temperatures of 35° , 40° , 45° , 50° , 55° and 60°C .

The oxide thickness was measured using an ellipsometer. The dimensions of the etched grooves were measured using a Leitz ORTHOPLAN optical microscope with a micrometer screw for fine focusing. The microscope was equipped with a mechanical stage with micrometer screws graduated for adjustment in X and Y directions.

The etch rate of the $\{111\}$ planes was determined from measurement of the oxide overhang on the base hole in the Si surface [28]. The transparent oxide mask allowed for simultaneous viewing of the original pattern boundary and the final groove wall boundary.

The slope of the groove walls was measured microscopically by comparing the positions required for sharp focus at different points on the wall [5]. A number of observation were made by Scanning Electron Microscope (SEM) and some photographs were taken. The wafer thicknesses were measured by micrometer.

The values cited below are mean values taken from the measurement of 10 samples at each temperature.

3. EXPERIMENTAL RESULTS AND DISCUSSION

The etch rates, R , of the silicon in $\langle 100 \rangle$ and $\langle 111 \rangle$ crystallographic directions in the temperature range 35° – 60°C are shown in Fig 1. The SiO_2 etch rate and the etching ratio of Si in the $\langle 100 \rangle$ direction to that of SiO_2 are also plotted in the same figure.

On the basis of these experimental data, it was approximately calculated that when a $400 \mu\text{m}$ thick wafer is used to obtain a $0.30 \mu\text{m}$ thick diaphragm an oxide of $\sim 0.8 \mu\text{m}$ and $\sim 0.3 \mu\text{m}$ thick is sufficient to protect the surface from etching with 35% KOH at 60° and 30°C , respectively.

According to Palik *et al.* [25], the etch rates of Si for the principal anisotropic etching solutions such as KOH, ethylenediamine and hidrazine, follow the sequence $R\{100\} \approx R\{110\} \gg R\{111\}$. Kendall [20] reported that the etch rates for KOH- H_2O mixtures follow the sequence $R\{110\} > R\{100\} > R\{111\}$. He found for 44 wt% KOH: H_2O at 60°C $R\langle 110 \rangle \approx 0.95 \mu\text{m}/\text{min}$. For the same temperature and 34% KOH we found $R\langle 100 \rangle \approx 0.33 \mu\text{m}/\text{min}$, which is in qualitative agreement with his observations. Weirauch [26] etched both spheres and slices of Si using 40 wt% KOH- H_2O and found the etch rate at 62°C around the $\{111\}$ plane along the $[110]$ zone. He found $R\langle 100 \rangle \approx 0.26 \mu\text{m}/\text{min}$. Under

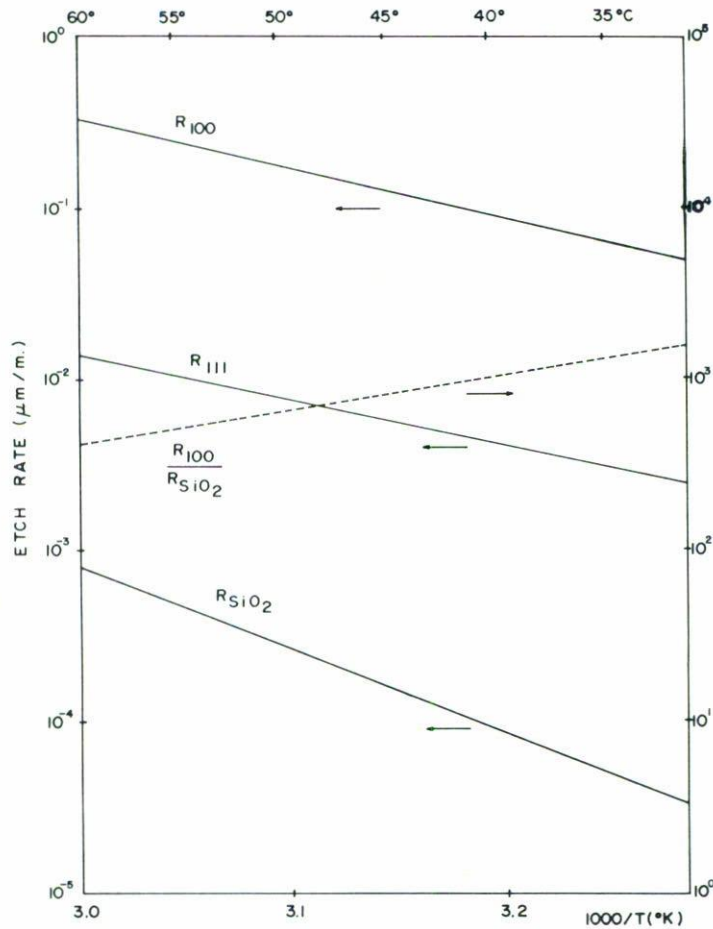


FIGURE 1. Etch rates of SiO₂ and Si in $\langle 100 \rangle$ and $\langle 111 \rangle$ direction in 34% KOH at different temperatures.

our experimental conditions and for $T = 60^\circ\text{C}$ we obtained $R\langle 100 \rangle \approx 0.33 \mu\text{m}/\text{min}$. The small difference in the temperature can not explain the difference in the etch rates whose ratio is 0.78. This difference can be explained taking into account the fact that the etch rate of KOH-H₂O for $\langle 100 \rangle$ Si increases with the increase of KOH concentration up to $\approx 22\%$ and then decreases. According to the published data [20] the ratio $R(40\%)/R(34\%) = 0.72$ at 30°C . Taking into account the difference in the temperatures, and probably in the experimental conditions, the agreement is fairly good.

Another important parameter of anisotropical Si etching is the rate ratio between the different crystallographic planes. Using a mixture of KOH, H₂O and isopropyl alcohol, Waggener *et al.* [29] have found etch rates for the $\langle 100 \rangle$ direction about 25 times faster than those in the $\langle 111 \rangle$ directions. According to Weirauch [26] this ratio is of the same order at 62°C . We found for our experimental conditions and for $T = 60^\circ\text{C}$ $R\langle 100 \rangle$:

$R\langle 111 \rangle \approx 26 : 1$. On the other hand, Kendall reported, based on an indirect study [24], that this ratio can be 200 : 1. However, the uncertainty in this case is of at least 10% [20].

For the case of SiO_2 , we found $R(\text{SiO}_2) \approx 8 \times 10^{-5} \mu\text{m}/\text{min}$ for 34wt% KOH at 40°C. For the same temperature and for 44 wt% KOH Kendall [20] reported $9.5 \times 10^{-5} \mu\text{m}/\text{min}$. According to the same author, the etch rate of thermally grown SiO_2 in KOH- H_2O is variable and depends on etching container and age of the solution, as well as on other factors.

Due to the backside anisotropic etching, pyramidal grooves were obtained as is shown in Fig. 2. Looking at these grooves amplified with a SEM we observe, in some cases, ledges on the walls of the grooves which start from the surface and go to the bottom of the grooves. As can be seen in Fig. 3, the ledges are not always straight lines, but present many steps and kinks. According to the literature [20, 23] these ledges are due to misaligned windows openings in the SiO_2 with respect to some low index crystallographic axes.

In our case the pattern geometry defined on the wafer surface, should be orthogonal to the $\langle 110 \rangle$ directions. Another effect of misaligning the opening in the oxide films is an increase in size of the etched hole in the Si substrate. The increase in size is caused by under etching of the oxide opening which enlarges the hole until its geometry is pinned to the nearest $\{111\}$ planes. According to our calculations, the misorientation of the mask with respect to the wafer flat in our case is $\approx 1.2^\circ$. The wafer flat is aligned to the true $\langle 111 \rangle$ plane within $\pm 1^\circ$ according to the vendor's specification. The misaligning of the oxide opening has a slightly less stringent effect for the $\langle 100 \rangle$ Si compared to the $\langle 111 \rangle$ one [27]. As can be seen from Fig. 1 for silicon, the etch ratio for the $\langle 100 \rangle$ directions to the $\langle 111 \rangle$ directions is almost constant in the present temperature range. This means that this misorientation is small, and can be due to the mask and/or wafer flat misorientation.

The other peculiarity was the following. After sufficient etching has occurred the hole in the surface is rectangular. It is bounded by four $\langle 111 \rangle$ planes, each of which makes an angle of 54.74° ($\arctan \sqrt{2}$) with the surface $\langle 100 \rangle$ plane [21]. We found that in some cases, this angle has a value greater than above, as is shown in Fig. 4.

At 35°C and 40°C this angle was found to be $\approx 58.19^\circ$ and $\approx 56.75^\circ$, respectively. For temperatures in the range 45–60°C and etching times longer than 18 hours we have measured 54.60° .

This value evidently coincides with the theoretical one of 54.74° within the range of the experimental error. Moreover this value can be used as a reference for the precision of our measurements.

This finding is of great importance for a better understanding of the anisotropic etching mechanisms as well as for the device technology.

The successful fabrication of many semiconductor devices with predictable characteristics requires precise control of their dimensions. For instance, the depth of the etched grooves is given by

$$d = \frac{W}{2} \tan \theta,$$

where W is the width of the mask opening and θ is the angle the appropriate $\langle 111 \rangle$ plane makes with the $\langle 100 \rangle$ surface plane. It is clear that small deviations from the theoretically

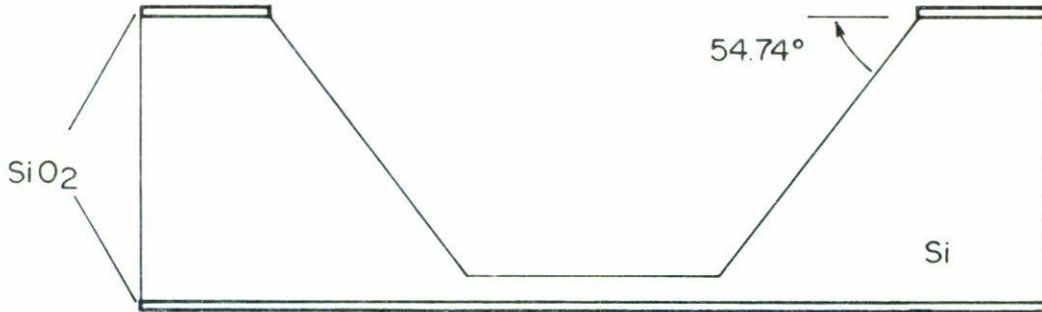


FIGURE 2. Schematic of the anisotropically etched groove.

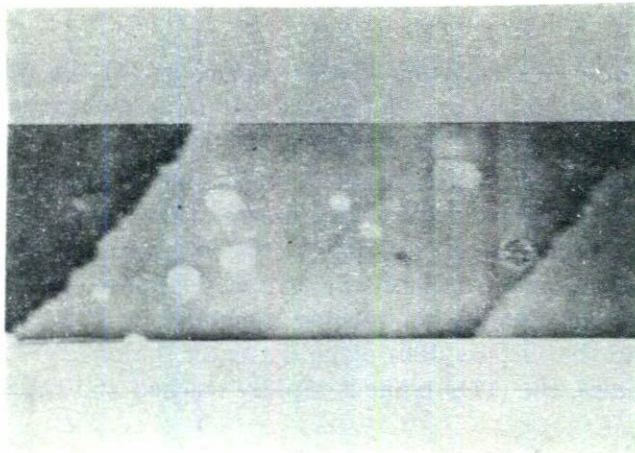


FIGURE 3. SEM view of ledges on the groove wall.

predicted value of 54.74° can produce important changes in the final dimensions of the groove.

Several reasons, such as misalignment in the opening in the oxide film, the presence of defects and mechanical stresses in the region near to the Si-SiO₂ interface, can be responsible for this effect. It has already been shown that the presence of defects and stresses increases the etch rate [20]. It is well known that during thermal oxidation of Si, defects are generated in the region near to the surface. On the other hand, due to the difference in the thermal expansion coefficients of Si and SiO₂ mechanical stress exists at the Si-SiO₂ interface.

Weirauch [26], who has etched mesas in (100) Si, found that for etching in directions off the [111], the slope of the mesa surface adjacent to the top masking oxide was steeper than expected. He proposes the hypothesis that this is due to: (i) the absence of a sharp

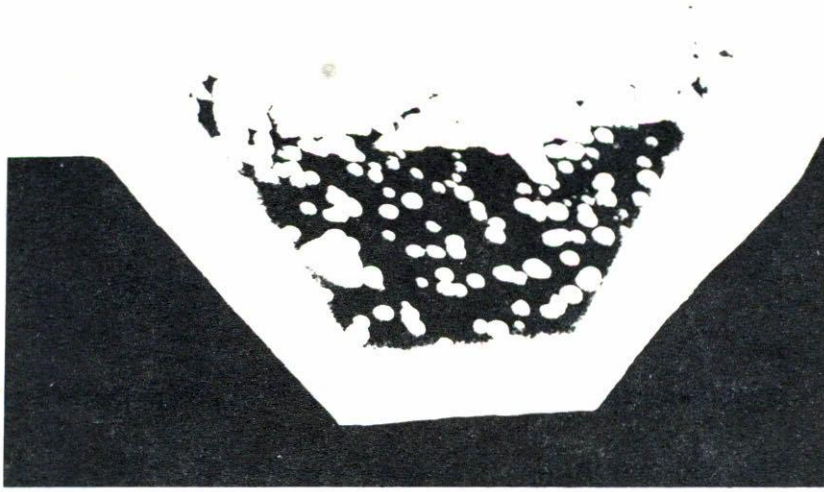


FIGURE 4. SEM view of a groove cut perpendicular to the bottom.

minimum in etch rate vs orientation in this region, or (ii) the relatively rapid rate of under cutting for these directions, which could alter the etchant composition under the etch mask sufficiently to modify the etching dynamics.

In our case we suppose that initially, due to mask and/or wafer flat misalignment, some high index planes are attacked with a rate greater than that of the $\{111\}$ planes. The increased etching rate, can be due not only to the misalignment but also to the presence of defects and stresses near the surface, and as it was supposed by Weirauch this can alter etchant composition and modify the etching dynamics. In this case, the angle between the groove walls and the surface (100) plane is greater than 54.74° . At high temperatures and long etching times, the (111) plane is rapidly reached and the measured angle is the predicated one.

4. CONCLUSIONS

The anisotropic etching of (100) oriented silicon wafers with 34% KOH in the temperature range $35^\circ\text{--}60^\circ\text{C}$ was investigated.

The Si etch rates in $\langle 100 \rangle$ and $\langle 111 \rangle$ directions, as well as this one for thermally grown SiO_2 were determined. The results are in agreement with expected ones. The minimum oxide thickness necessary to protect the diaphragm under the present experimental conditions was established.

It was found that the angle between the (111) walls of the etched grooves and the (100) surface plane can be greater than 57.74° .

Additional experiments to investigate this finding are necessary. Some other experiments are necessary to determine the etch rate of (100) Si at different KOH concentrations, since few data exists in the literature.

ACKNOWLEDGEMENT

The authors wish to thank I. Fuentes from the Microelectronics Department of INAOE for the SEM photos and SEP, and CONACYT for the partial support of this project.

REFERENCES

1. D.R. Turner, *J. Electrochem. Soc.* **105** (1958) 402.
2. B. Schwarts and H. Rabbin, *J. Electrochem. Soc.* **106** (1959) 505; **107** (1950) 108; **108** (1961) 365.
3. W.C. Dash, *J. Appl. Phys.* **27** (1956) 1193.
4. J.M. Crishal and A.L. Harrington, *Electrochem. Soc. Extended Abstract*, Spring Meeting. (1962), Los Angeles, C.A., Abstr. No. 89.
5. D.B. Lee, *J. Appl. Phys.* **40** (1969) 4569.
6. D.L. Spears and H.I. Smith, *Solid State Tech.* **15** (1972) 21.
7. D.L. Spears and H.I. Smith, *Electron Lett.* **8** (1972) 102.
8. P.V. Lenzo and E.G. Spener, *Appl. Phys. Lett.* **24** (1974) 289.
9. W.T. Tsang, C.C. Tseng and S. Wang, *Appl. Opt.* **14** (1975) 1200.
10. T.O. Sedgwick, A.N. Broers and B.J. Agule, *J. Electrochem. Soc.* **119** (1972) 1769.
11. E. Bassous, H.H. Taub and L. Kuhn, *Appl. Phys. Lett.* **31** (1972) 135.
12. D.A. Kiewit, *Rev. Sci. Instrum.* **44** (1973) 1741.
13. C.L. Huang and T. Yan Duzer, *IEEE Trans. El. Dev.* **ED-2** (1976) 579.
14. T.J. Rodgers and J.D. Meindl, *IEEE Trans. El. Dev.* **ED-20** (1973) 226.
15. M.J. Declereq, *IEEE J. Solid-State Circuits* **SC-10** (1975) 191.
16. H. Guckel, S. Larsen, M.G. Lagally, G. Moore, J.B. Miller and J.D. Wiley, *Appl. Phys. Lett.* **31** (1977) 618.
17. K.E. Peterson, *Appl. Phys. Lett.* **31** (1977) 521.
18. O.N. Tufte, P.W. Chapman and D. Long, *J. Appl. Phys.* **33** (1962) 3322.
19. K.E. Peterson, *Proc. IEEE* **20** (1982) 420.
20. D.L. Kendall, *Ann. Rev. Mater. Sci.* **9** (1979) 373.
21. E. Bassous, *IEEE Trans. El. Dev.* **ED-23** (1978) 1178.
22. D.L. Kendall, *Appl. Phys. Lett.* **26** (1975) 195.
23. E.A. Lewis and E.A. Irene, *J. Electrochem. Soc.* **134** (1987) 2332.
24. D.L. Kendall, *J. Vac. Sci. Technol.* **A8** (1990) 3598.
25. E.D. Palik, V.M. Bermudez and O.J. Glembocki, *J. Electrochem. Soc.* **132** (1985) 871.
26. D.F. Weirauch, *J. Appl. Phys.* **46** (1975) 1478.
27. K.E. Bear, *IEEE Trans. El. Dev.* **ED-25** (1978) 1185.
28. E. Bassous and E.F. Baron, *J. Electrochem. Soc.* **125** (1978) 1321.
29. H.A. Waggner, R.C. Kragness and A.L. Tyler, *Electronics* **40** (1967) 274.