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Influence of the oxide traps on the pulse MOS C-t measurements

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ABSTRACT. For some n-type MOS structures measured by the pulse MOS C-t technique at different temperatures; it was found that the initial capacitance increases with the increase of temperature when negative pulses of the same amplitude are applied. This effect was found to be due to a hole trapping in the oxide and interface traps. It is shown how this trapped charge can be measured using pulse MOS C-t technique.

RESUMEN. Se encontró que para algunas estructuras MOS tipo n, medidas con el método MOS C-t, a diferentes temperaturas, el valor de la capacitancia inicial aumenta con la temperatura para pulsos de voltaje negativos de la misma amplitud. Este efecto se explica como atrapamiento de huecos en las trampas en el óxido. Se muestra cómo esta carga puede ser medida usando la técnica MOS C-t pulsada.

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1. INTRODUCTION

Continuous material improvement and process optimization have resulted in silicon devices with very high generation lifetime (> 1 ms). Generation lifetime measurement in high quality materials is a major problem because a single measurement using pulse MOS C-t (metal-oxide-semiconductor capacitance-time) methods can take several minutes even hours. To reduce the measurement time it was proposed to use high temperatures [1,2]. On the other hand there are pulse MOS C-t methods which use high temperatures to measure the recombination lifetime [3].

In the course of pulse MOS C-t measurements, at different temperatures, we found that for some n-type MOS structures the value of the initial capacitance (the capacitance at $t = 0^+$ after applying the voltage pulse) increases with the increase of temperature when negative voltage pulses, with the same amplitude, are applied.

The aim of this paper is to demonstrate experimentally this effect and to show that it is due to a hole trapping in the oxide. Moreover, it has been shown how the pulse MOS C-t technique can be used to measure the oxide trapped charge.

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2. THEORY

Let us consider a MOS capacitor with ionized donors concentration N_D in the substrate. If at the moment $t = 0$ a voltage pulse V_G is applied to the field electrode we can write

$$V_G = V_{ox} + \phi_s + V_{FB}, \tag{1}$$

where V_{ox} is the voltage drop in the oxide, ϕ_s is the surface potential and the flat band voltage is given by

$$V_{FB} = \phi_{ms} - \frac{Q_f + Q_{ot} + Q_{it} + Q_m + Q_p}{C_{ox}}, \tag{2}$$

where ϕ_{ms} is the metal-semiconductor work function difference, Q_f is the fixed oxide charge density, Q_{ot} is the oxide trap charge density, Q_{it} is the fast surface state density, Q_m is the mobile ions charge density, Q_p is the surface charge induced by the dipole polarization, and C_{ox} is the oxide capacitance.

To find V_{ox} we proceed as follows. Under a strong inversion condition the charge per unit area in the semiconductor is given by

$$Q_s = Q_i + Q_{sc} = Q_i + qN_D W, \tag{3}$$

where Q_i is the inversion layer charge per unit area, Q_{sc} is the space charge per unit area, q is the charge of electron and W is the depletion layer width. Q_i and Q_{sc} are positive quantities for n-type substrate and negative for p-type substrate.

The voltage drop in the oxide is given by

$$V_{ox} = \frac{Q_s}{C_{ox}} = \frac{Q_i + Q_{sc}}{C_{ox}}. \tag{4}$$

Neglecting the voltage drop in the inversion layer we have

$$V_{ox} = \frac{Q_{sc}}{C_{ox}} = \frac{qN_D W}{C_{ox}}. \tag{5}$$

Now we need to find ϕ_s. In the case of deep depletion the charge is written as

$$\rho = qN_D, \quad \text{for} \quad 0 \le X \le W. \tag{6}$$

The solution of the Poisson's equation with the boundary condition of $E = 0$ and $\phi = 0$ at $X = 0$ gives the electric field

$$E(x) = \frac{qN_D(W - X)}{\epsilon_0 \epsilon_s}, \quad \text{for} \quad 0 \le X \le W, \tag{7}$$

where ϵ_0 and ϵ_s are the permitivity of the free space and the dielectric constant of silicon, respectively.

Integrating a second time we obtain the potential variation with X:

$$\phi(x) = \frac{qN_D(W-X)^2}{2\epsilon_0\epsilon_s}, \quad \text{for} \quad 0 \leq X \leq W, \tag{8}$$

and the surface potential at $X = 0$ is given by

$$\phi_s = \frac{qN_D W^2}{2\epsilon_0\epsilon_s}. \tag{9}$$

Substituting (2), (5) and (9) in (1) we obtain

$$V_G = \frac{qN_D W}{C_{ox}} + \frac{qN_D W^2}{2\epsilon_0\epsilon_s} + \phi_{ms} - \frac{Q_f + Q_{ot} + Q_{it} + Q_m + Q_p}{C_{ox}}. \tag{10}$$

Using the relation

$$C_{sc} = \frac{\epsilon_0\epsilon_s}{W} = \frac{C_{ox}C}{C_{ox} - C}, \tag{11}$$

where C_{sc} is the space charge capacitance and C is the measured capacitance of the MOS structure, we obtain after some transformations from (10)

$$V_G = \frac{q\epsilon_0\epsilon_s N_D}{2C_{ox}^2}\left[\left(\frac{C_{ox}}{C}\right)^2 - 1\right] + \phi_{ms} - \frac{Q_f + Q_m + Q_{ot} + Q_{it} + Q_p}{C_{ox}}. \tag{12}$$

In the present case, as it is shown in Sect. 4, Q_m and Q_p can be neglected. At $t = 0^+$, $C = C_i$ and so we can write

$$V_G = \frac{q\epsilon_0\epsilon_s N_D}{2C_{ox}^2}\left[\left(\frac{C_{ox}}{C_i}\right)^2 - 1\right] + \phi_{ms} - \frac{Q_f + Q_{ot} + Q_{it}}{C_{ox}}, \tag{13}$$

where C_i is the initial capacitance illustrated in Fig. 1.

From (13) we can obtain the trapped charge $Q_T = Q_{ot} + Q_{it}$:

$$Q_T = C_{ox}\left\{\frac{q\epsilon_0\epsilon_s N_D}{2C_{ox}^2}\left[\left(\frac{C_{ox}}{C_i}\right)^2 - 1\right] + \phi_{ms} - V_G\right\} - Q_f. \tag{14}$$

If we apply on the MOS structure depleting voltage pulses of the same amplitude and as a result obtain different values for C_i then from (14) we can determine the change of the oxide traps charge $\Delta Q_T = Q_T^2 - Q_T^1$:

$$\Delta Q_T = \frac{q\epsilon_0\epsilon_s N_D}{2C_{ox}}\left[\left(\frac{C_{ox}}{C_{i2}}\right)^2 - \left(\frac{C_{ox}}{C_{i1}}\right)^2\right]. \tag{15}$$

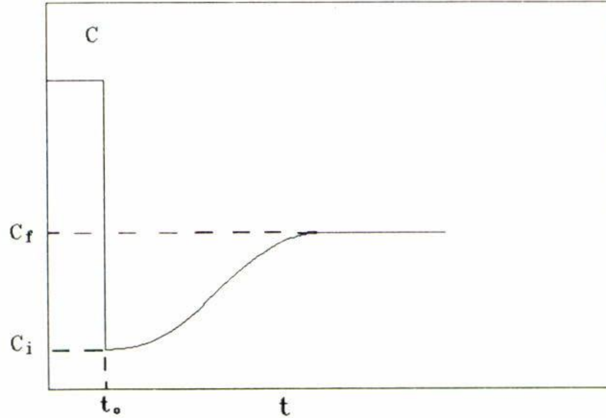

FIGURE 1. Schematic capacitance *versus* time curve.

From (13) we can obtain the initial capacitance as a function of the trapped hole charge:

$$C_{\rm i} = C_{\rm ox}\left[\frac{2C_{\rm ox}^2}{q\epsilon_0\epsilon_{\rm s}N_{\rm D}}\left(V_{\rm G} - \phi_{\rm ms} + \frac{Q_{\rm f} + Q_{\rm ot} + Q_{\rm it}}{C_{\rm ox}}\right) + 1\right]^{-1/2}. \tag{16}$$

As it can be seen from (16) with the increase of the trapped positive charge ($Q_{\rm ot} + Q_{\rm it}$) the initial capacitance $C_{\rm i}$ increases (negative $V_{\rm G}$).

3. SAMPLES PREPARATION AND MEASUREMENTS

The MOS capacitors were made on Czochralski grown Si substrates with (100) orientation. The n-type substrates were phosphorus doped with resistivity 2-5 ohm-cm. All wafers were cleaned by the standard RCA process. The wafers were oxidized in dry O_2 + 2% TCA at $T = 1000°$C to oxide thickness 770 Å. After the oxidation all wafers received thermal treatment in N_2 at $T = 1000°$C for 30 min.

High purity aluminum was evaporated through a metal mask to form the gate electrodes. The backside oxide was removed and aluminum was evaporated for a back contact. Finally, the wafers received a post-metallization anneal in forming gas (N_2/H_2 ambient) at $T = 400°$C for 30 min.

Capacitance *versus* voltage and capacitance *versus* time measurements of the MOS structures were done at 1 MHz frequency. In the last case the devices were pulsed from 0 to -5 V at different temperatures.

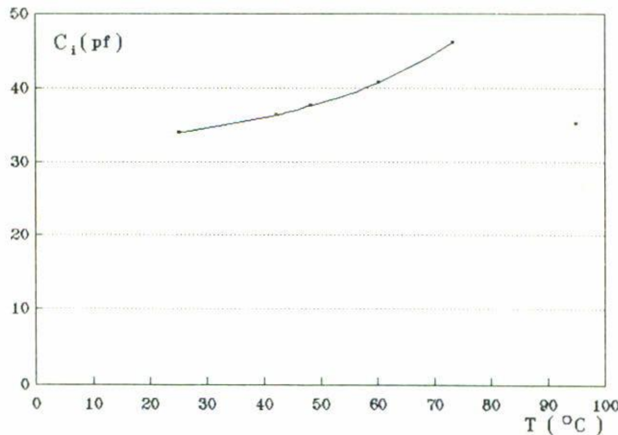

FIGURE 2. Initial capacitance *versus* temperature. At every temperature a voltage pulse with -5 V amplitude was applied on the MOS structure.

4. Experimental results and discussion

The change of the initial capacitance $C_{\rm i}$ as a function of temperature for one of the samples is shown in Fig. 2. The area of the metal electrode for that sample was 10^{-2} cm^2. Only one pulse was applied on the MOS capacitor for a given temperature. The amplitude was -5 V. The duration of the pulses was different at different temperatures. A C-V shift along the voltage axis, due to the trapped positive oxide charge, correlating with $C_{\rm i}$ change, was observed.

It can be seen from Fig. 2, that the initial capacitance increases with the temperature after applying a voltage pulse. This means that the electric field penetration in the semiconductor decreases. For an ideal MOS structure [$V_{\rm FB} = 0$, see Eq. (1)] the value of the initial capacitance depends on the applied voltage, the concentration of the ionized impurity atoms in the space charge region (SCR) $N_{\rm D}$ and the oxide thickness [see Eq. (10)]. All these three parameters are constant for a given MOS capacitor and do not depend on the bias-temperature (B-T) stress. In the case of real MOS structure ($V_{\rm FB} \neq 0$), according to Eq. (2), the parameters which can be influenced by the B-T stress are oxide traps charge, interface traps charge, mobile ions charge and the surface charge due to the dipole polarization. The effect of the slow trapping is similar to the negative bias stress effect. That is why in the present case the charge in the slow traps is included in the oxide traps charge $Q_{\rm ot}$ [Eq. (2)], but the effect of the slow oxide traps in this experiment is doubtful. The charge in the slow oxide traps may leave away even at room temperature. In our case the time between two subsequent measurements was relatively long and the temperature was high. On the other hand at room temperature measurements, it was not observed a hysteresis of the C-V curves, corresponding to a charge exchange with the slow oxide traps or to any other type of instability.

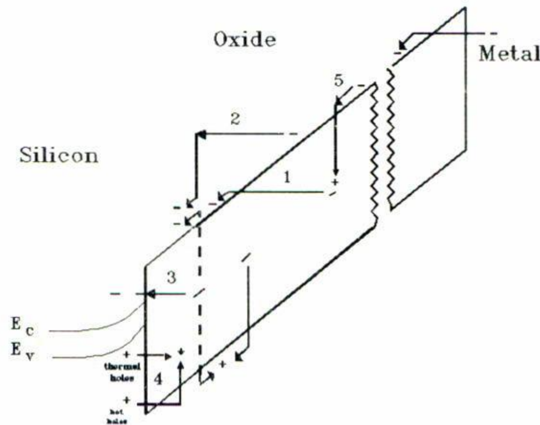

FIGURE 3. Band diagram illustrating the mechanisms of hole trapping.

According to Fig. 2 the behavior of the initial capacitance is the reversal of that corresponding to the mobile ion instability and to the dipole polarization. This means that the only explanation of the C_i change due to the negative B-T stress is the hole trapping by the bulk oxide traps and by the interface traps. The last ones also can contribute to the hole trapping [4].

Because the aim of this article is to demonstrate the influence of the hole trapping on the pulse MOS *C-t* measurements and the way to measure the trapped charge by this technique, we will only discuss in brief the trapping mechanisms.

The hole trapping mechanism, which is often referred as the negative-bias instability, was described first by Nicollian [5].

One of the methods of creating trapped holes is to apply large negative fields on the gate of a MOS structure [6,7]. Normally, the effect of the hole trapping is investigated by the measurement of the injection current, flat band voltage shift or the shift of threshold voltage of MOS transistors

In spite of the fact that it is still not clear which is the dominant trapping process at given experimental conditions, there are several proposed mechanisms which are illustrated in Fig. 3.

Process (1) [8] is the direct tunneling of an electron from a neutral trap into the oxide conduction band. It is supposed that this is the dominant mechanism at very high electric fields.

Process (2) [9] is due to creation of an electron-hole pair by impact ionization of a hot electron, injected at the gate electrode. The hole could then be trapped, and the electron leaves the oxide and adds to the oxide current.

Process (3) [8] represents direct tunneling of an electron from a neutral trap into the silicon conduction band. This mechanism depends on the trap energy level and is limited

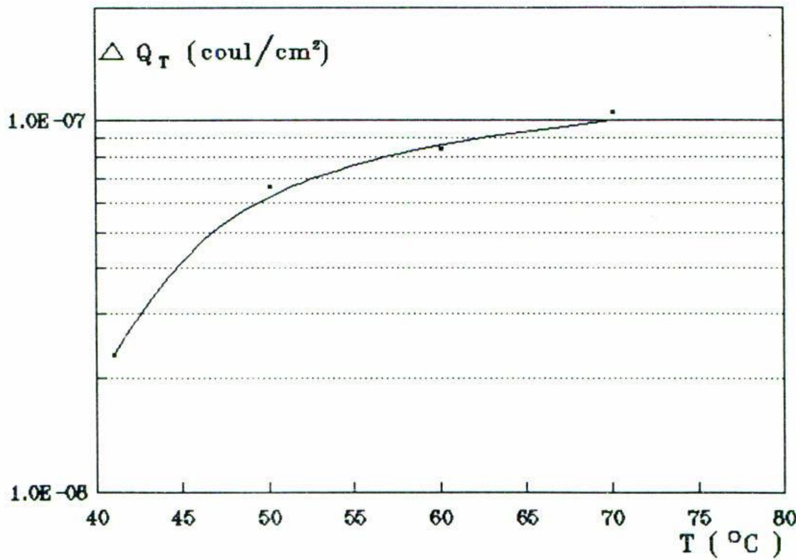

FIGURE 4. Hole trapped charge *versus* temperature.

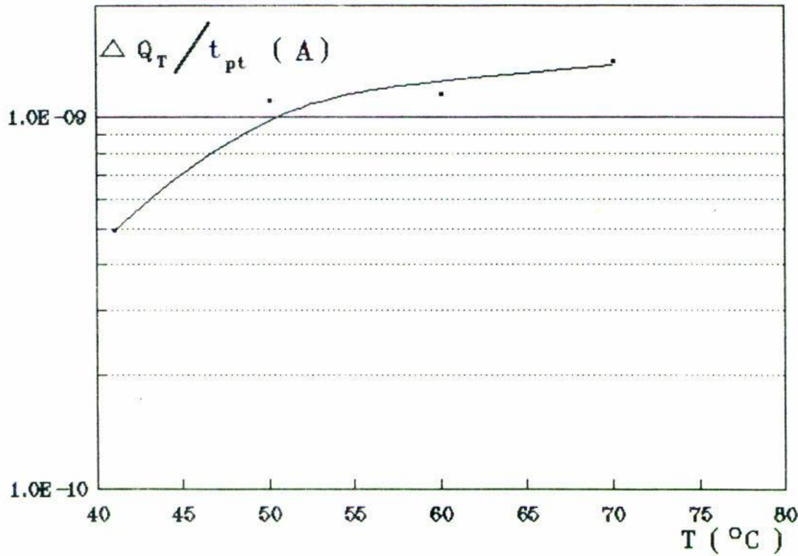

FIGURE 5. Hole current *versus* temperature.

to traps located close to the interface. Partial de-trapping is quite possible and it is thought that this mechanism is not the most significant during B-T stress.

Process (4) is the tunneling of holes from the silicon valence band into the SiO_2 valence band, from where they are trapped. This mechanism is similar to that proposed by Hofstein [10]. According to Weinberg [11] in this process can participate as thermal as hot holes.

Process (5) can be considered as neutralization of the trapped holes by conducting electrons at high fields.

The nature of the hole traps is normally related with extrinsic defects such as Si–H or Si–OH bonds or intrinsic ones as Si–O bonds which are stretched or disturbed. New traps can also be created by the action of a B-T stress [6,8,12,13]. Also it is known that when oxides are grown in HCl–containing ambient, relatively large positive interface charge builds up during a subsequent negative B-T stress [14,15].

Using Eq. (15) and the results from Fig. 2 we calculated the total positive trapped charge ΔQ_{T} accumulated after every B-T stress cycle. The result is presented in Fig. 4. Dividing the total accumulated oxide trapped charge after each B-T stress cycle to the total B-T stress time, the effective hole current was obtained. The result is presented in Fig. 5.

Here it must be mentioned that during the time between two measurements, necessary to increase the temperature, it is quite probable that some small part of the trapped holes are released from the traps.

5. Conclusions

During the pulse MOS *C-t* measurements, especially at elevated temperature, a quasi-stationary charge can be built-up in the oxide and to screen the bulk of semiconductor from the applied electric field. Experimental results, demonstrating this effect and its influence on the MOS *C-t* characteristics, are presented. Brief review of the existing models explaining this type of charge instability is given. A theoretical base, which explain the experimental results is presented and a method using the pulse MOS *C-t* technique, to measured this charge is proposed.

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References

1. W.R. Fahrner, D. Braeuning, C.P. Schneider and M. Briere, *J. Electrochem. Soc.* **134** (1987) 1291.
2. Z. Radzimski, E. Gaylord, J. Honeycutt and G.A. Rozgonyi, *J. Electrochem. Soc.* **135** (1988) 2597.
3. D.K. Schroder, J.D. Whitfield and C.J. Varker, *IEEE Trans. El. Dev.* **ED-31** (1984) 462.
4. S.K. Lai and D.R. Young, *J. Appl. Phys.* **52** (1982) 6231.
5. E.H. Nicollian, *Proc. 12th Ann. IEEE Rel. Phys. Sump.* (1974) p. 267.
6. K.O. Jeppson and C.M. Svensson, *J. Appl. Phys.* **48** (1977) 2004.
7. D.J. Di María, Z.A. Weinberger and J.M. Aitken, *J. Appl. Phys.* **48** (1977) 898.
8. M.H. Woods and R. Williams, *J. Appl. Phys.* **47** (1978) 1082.
9. T.H. Distefano and M. Shatzkes, *J. Vac. Sci. Tech.* **13** (1976) 40.

10. S.R. Hofstein, *Sol.- State Electron* **10** (1967) 657.
11. Z.A. Weinberg, W.C. Johnson and M.A. Lampert, *J. Appl. Phys.* **47** (1976) 248.
12. A.G. Revez, *J. Non-Cryst. Solids* **11** (1973) 309.
13. I. Kobayashi, M. Nakahara, and M. Atsumi, *Proc. IEEE* **61** (1973) 249.
14. B.P. Rai and R.S. Srivastava, *J. Phys. D.* **11** (1978) 2139.
15. S. Iwamatsu and Y. Tarui, *J. Electrochem. Soc.* **126** (1979) 1078.