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Investigation of process-induced contaminations in silicon wafer processing

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ABSTRACT. Contaminations introduced by some semiconductor fabrication processes such as wet oxide etching, lithography and high temperature annealing were investigated by the MOS C-t technique. It is shown that these processes can deteriorate generation lifetime. It is supposed that during wafer processing, Si wafers are contaminated with metallic impurities. During the high temperature process steps these impurities diffuse into the Si affecting the generation lifetime. The sources of metallic contamination are discussed.

RESUMEN. Se investigó, usando la técnica MOS C-t, la contaminación introducida por etapas de proceso tales como: grabado húmedo de óxido, litografía y recocidos a alta temperatura. Se demuestra que esos procesos pueden deteriorar el tiempo de vida de generación. Se cree que durante el proceso de fabricación de circuitos integrados las obleas se contaminan con impurezas metálicas. Durante los procesos de alta temperatura, estas impurezas se difunden en el silicio, afectando el tiempo de vida de generación. Se discuten las fuentes de la contaminación metálica.

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1. INTRODUCTION

The advance in IC (integrated circuit) complexity during the last 15 years have resulted in a 200× increase in the number of transistors per die. The most important factor in achieving such complexity is the continued reduction of the minimum device dimensions. Now, we are approaching ULSI (ultra large scale integration), and this opens the door to nanoprocess engineering whose focus us on the detailed atomic-scale properties of the device structure. As a result of this tendency, it is becoming more critical to control and minimize the impurities and crystalline defects in the starting material as well as these one introduced during IC fabrication processes. The scaled down devices are proved to be more sensitive to any kind of defects and contaminations. The increased number of studies investigating the sources of contamination during Si wafers processing reflects the importance of the problem.

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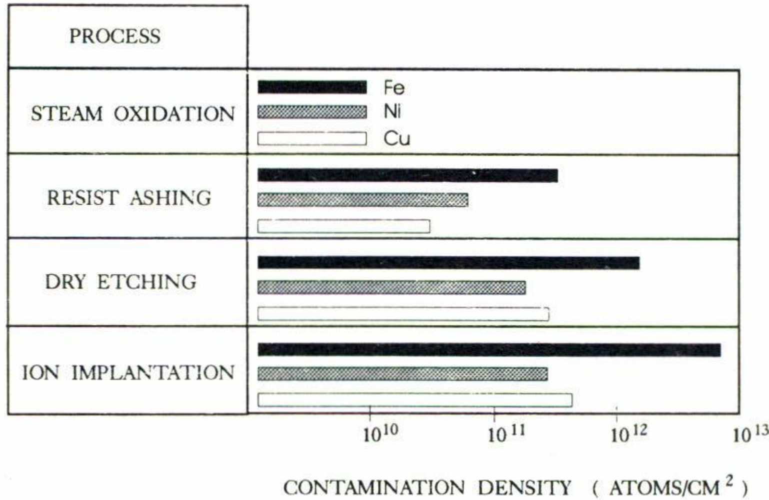

FIGURE 1. Metallic impurities on silicon wafer surface from actual dry processing, Ref. [9].

Metals, originating from chemicals [1,2], gas lines [3,4], gas sources [5], dopant materials [6] or processing equipment [3], can contaminate Si wafers during different process steps.

Metallic contaminants are responsible for providing nucleation sites for the generation of stacking faults (SF). On the other hand, it is well known that some metals such as Au, Cu, Zn, Co, Cr, Mn, Fe, Ni, Pt, Mo and Ag introduce energy levels in the band gap of Si. Some of these levels are deep ones and appear to be effective generation-recombination centers, which affect strongly the generation lifetime, *i.e.*, the average time necessary to generate an electron-hole pair. For instance, Au, Cu, Cr, Zn and Fe introduce $E_C - 0.54$, $E_V + 0.52$, $E_C - 0.41$, $E_C - 0.55$ and $E_C - 0.51$ eV levels, respectively [7]. Part of these metals are known as fast diffusers. They decorate the SF and other crystalline defects affecting by this way their electrical activity. The metallic contamination of Si can cause fatal effects on semiconductor devices such as increase the leakage current at the p–n junctions, decrease the oxide breakdown voltage, and deterioration of the carrier lifetime. It has been recognized that metallic contamination is a leading yield hundrance [3], and must be suppressed to less than 1×10^{10} atom/cm^2 in order to prevent the above mentioned effects [8]. However in the current processes, the contamination on the Si wafer cannot be reduced to less than 10^{12} atom/cm^2, as is shown in Fig. 1 [9].

In the present work the metallic contamination introduced during oxide etching, photolithography and post-gettering annealing was investigated. Generation lifetime was chosen as the measurable parameter for detecting metallic impurities, which could be introduced during these process steps, because it is more sensitive to them, compared with the chemical or physical trace analysis methods [3].

TABLE. Principal process steps for each wafer.

	Process	Wafer				
		E4	E2	E3	E1	E5
A	Back oxide etching with BOE. Top oxide protected by photoresist.			×	×	
B	Back oxide etching manually with HF.	×	×			×
C	Backside phosphorus ion implantation.	×	×	×	×	×
D	Partial oxide etching with $HF + NH_4F + H_2O$.		×		×	
E	Annealing in cleaned furnace.	×	×	×	×	
F	Annealing without cleaning the furnace.					×

2. SAMPLES PREPARATION AND MEASUREMENTS

In this experiments n–type, (100) oriented, 2.5–5 ohm-cm, CZ grown Si wafers were used. First, all wafers were ultrasonically and RCA SC1 (NH_4OH:H_2O_2:H_2O) + SC2(HCL: H_2O_2:H_2O)) [10] cleaned. The RCA cleaning is believed to be efficient in removing contaminants on the substrate surface such as particles, organic materials and metallic impurities [11]. The wafers were oxidized in dry O_2 + 2% TCA ($C_2H_3Cl_3$) ambient at 1000 °C to obtain 800 Å thick oxide. Immediately after the oxidation they were annealed at the same temperature in dry N_2 for 30 min. The subsequent process steps were different for the different wafers and they are presented in the Table.

In the case of process A (see the Table) the top oxide was protected with negative photoresist KTI 747R, during the back oxide etching. The back oxide was etched using BOE (buffered oxide etchant) (HF: (NH_4:H_2O) 1:7 (KTI Chemicals Inc.) The photoresist was developed using "Xilene" (J.T. Baker) as a developer followed by 30 sec in 2-propanol. The photoresist removal was done in H_2SO_4: H_2O_2 7:2 solution. After that, the wafer was rinsed in DI (deonized wafer), RCA cleaned and rinsed again in DI till resistivity of 18 Mohm-cm was reached.

Process B was used to remove the backside oxide, using a HF wet cotton, supposing that in this case the top surface of the wafer will be kept uncontaminated.

Process D was designed to remove metallic contamination due to the ion implantation, by etching part of the top oxide, as it is recommended [11]. The oxide was partially etched in BOE.

The purpose of the experiment with processes E and F was to check if the high temperature nitrogen annealing introduces contaminations, and if they can be gettered. In both cases the annealing was performed at 900 °C for a long time (150 min.) to permit the effect of the contamination (if exists) to be noted. In the case of process E, before the annealing the furnace was cleaned by dry O_2 + TCA flux during 2 hours at 1100 °C. The process F was performed without preliminary cleaning of the furnace.

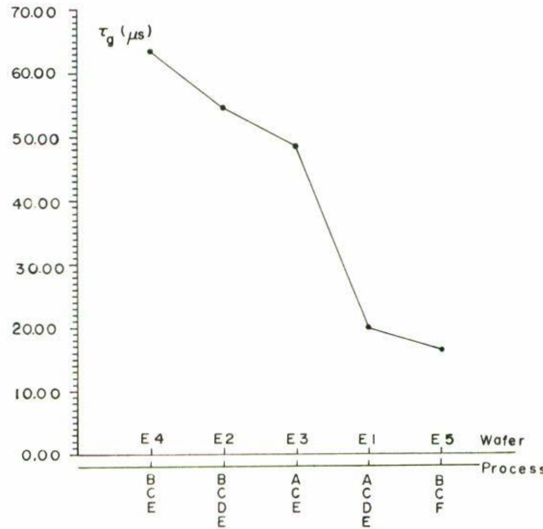

FIGURE 2. Generation lifetime as a function of process steps.

The final process steps for all wafers were Al evaporation on the top oxide through a metal mask, Al evaporation on the backside of the wafers and sintering. The sintering was performed in N_2/H_2 ambient at 425 °C for 30 min.

MOS C-t measurement at 1MHZ were performed to determine the generation lifetime, using the modified Zerbst method [12]. Ten capacitors of each wafer were measured and the average value of the generation lifetime for each wafer was calculated.

3. EXPERIMENTAL RESULTS AND DISCUSSION

In Fig. 2, the change in generation lifetime, τ_g due to the different process steps is shown. The highest generation lifetime measured, was in the wafer #4. Looking at Fig. 2 and at the Table, in which the different process steps are described, it can be noted that the measured generation lifetime decreases with the increase of the number of process steps as well as due to some specific process steps. The decrease in τ_g for each case is explained as follows.

The decrease of τ_g in wafer #2 can be explained in view of the results of Hsu *et al.* [2], which have investigated the metallic contamination resulted from the use of HF-based solutions. The particular process of wafer #2, includes the use of a HF-based solution to remove metallic contamination, due to the ion implantation, as it was recommended [13]. When one compares the results obtained for this wafer with the results of wafer #4 (which has not been treated by this way) it is evident that the decrease in τ_g is due to the cleaning process (process D), supposed to be used to remove metallic contamination. In Ref. [2] the contaminants arising from the HF-based solutions were identified as Cu, Au, Mo and Ag.

As can be seen from the same figure, the use of process A, with respect to wafer #3, resulted in a greater decrease of τ_g. In this case the situation is much more complex because the use of a photoresist includes many process steps such as photoresist deposition, development and stripping as well as other intermediate steps (baking, exposing, rinsing, etc.). It is evident that with the increase of the number of process steps the probability of contamination increases. Meanwhile the photoresist alone is responsible for organic contamination [14], some of the manipulations and solutions used in process A can be responsible for metallic contamination. For instance, the back surface of the wafers when in contact with the metallic chuck during photoresist deposition and spinning are contaminated with metallic particles. The particles can be transferred to the front-surface of the wafers in the cleaning solutions and during thermal processing —so called back-surface contamination [15].

It was normally thought that RCA cleaning was enough to remove metallic contamination, but critics of this cleaning procedure have pointed out some drawbacks of its use. For example, SC1 solutions leaves considerable contamination of Fe [16,17], Zn [16] and Al [18]. On the other hand, even that SC2 solution was designed to remove the metals, it also can be source of metallic contamination, for instance Fe [17]. At present there is not a complete cleaning sequence which insure total removal of all metals from the Si surface. It has also been reported that RCA cleaning as well as other basic cleaning procedures can not remove Ni from the Si surface (if contaminated) [19]. Evidently the use of processes A and D, identified already as sources of contaminations, provokes much more deterioration of generation lifetime, (wafer #1, processes A, C, D and E), as it can be seen in Fig. 2.

Finally the greatest deterioration of the generation lifetime is manifested in wafer #5, due to the annealing in uncleaned furnace (process F). It has already been reported that metallic contamination can be introduced by different high temperature processes [20,21]. For instance, during special investigations high amount of impurities such as Cu, Na, Ni, Fe, Cr, Al, Ti and Mg, were detected in the oxidation furnace tube, especially close to the mouth [22].

4. Conclusions

Contaminations introduced during wet oxide etching, lithography and long-time high temperature annealing were investigated by the measurement of generation lifetime in MOS structures. It has been shown that these processes can contaminate Si wafers with metallic impurities, which diffusing into the Si deteriorate generation lifetime. It is supposed that the main sources of metallic contamination for wet oxide etching and lithography processes are the chemicals used. It is evident that there is need of cleaner chemicals. Thus, identifying the sources of contamination can help to reduce or eliminate them. In the long run, it is expected that wet cleaning and etching methods will be totally replaced by vapor and dry ones [16].

In the case of high temperature annealing the contamination is due to the furnace and/or incoming gas contaminations. The use of clean furnace tubes, lower temperatures, ramping after high temperature process, pure gases and chemicals can reduce or avoid the contaminations.

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