

Influence of process sequence on the P ion implantation gettering efficiency

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ABSTRACT. P ion implantation gettering efficiency in MOS structures as a function of the process sequence was investigated. It has been found that a gettering performed after an oxidation results in higher generation lifetime and lower surface generation velocity compared with the one performed before the oxidation. It is supposed that ion implantation process is a source of metallic contamination. When the implantation is performed before the oxidation, the top wafer surface is not protected and heavy metals penetrate easier into the bulk of silicon. This results in inferior generation lifetime and surface generation velocity. The subsequent thermal annealing improves these parameters, but cannot eliminate totally the effect of contamination.

RESUMEN. Se investigó la eficiencia de *gettering* por implantación iónica de fósforo como función de la secuencia del proceso de fabricación. Se encontró que el *gettering* efectuado después de una oxidación tiene mayor tiempo de vida de generación y menor velocidad de generación superficial, comparada con uno hecho antes de la oxidación. Suponemos que la implantación es una fuente de contaminación metálica. Cuando la implantación es efectuada antes de la oxidación, la superficie de la oblea queda desprotegida y es más fácil que metales pesados penetren, dando por resultado un tiempo de vida y una velocidad de generación superficial inferior. Tratamientos térmicos posteriores pueden mejorar estos parámetros, pero no eliminan totalmente el efecto de la contaminación.

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1. INTRODUCTION

Semiconductor devices are especially susceptible to contaminations during the fabrication process. These contaminations affect directly the manufacturing yield, the performance and the reliability of IC's. Principal sources of contamination are the people, facility, tools, chemicals and materials used for clean room construction. There are different kind

of contaminations such as organic, metallic, etc. A source of the organic contamination is normally people and liquid chemicals [1]. Potential sources of the metallic contamination are stainless steel gas lines [2,3] (due to the corrosion by a moisture introduced accidentally to the HCl, TCA or TCE lines), the metallic tweezers and the metallic parts of some equipments [3,4].

Among all kinds of contaminations this one due to the metallic impurities is the most harmful because it affects oxide breakdown voltage and device leakage current.

To remove unwanted metallic impurities from the device active region of the wafers various gettering techniques are widely used [5,6,7]. Taking into account that some process steps can be responsible for the contamination as well as the peculiarities of the gettering process, it is very important to program the gettering process at a specific point in the process sequence.

One of the critical process steps in the fabrication of MOS IC's is the gate oxide growth. This process influences the surface, as well the bulk properties of semiconductor devices. That is why it is important to know the place of gettering in the process sequence and specially with respect to the oxidation.

In the present work, the efficiency of the P ion implantation gettering performed before and after the oxidation was investigated. The gettering efficiency was evaluated by the generation lifetime and surface generation velocity measurements in MOS capacitors. It is well known that the method of generation lifetime measurements is more sensitive to the metallic impurities compared with the physical and chemical trace analysis methods [8].

2. SAMPLES PREPARATION AND MEASUREMENTS

N-type, (100) oriented, 2.5–5 ohm-cm silicon wafers were used in this experiment. All wafers were cleaned and divided in two groups, A and B. The wafers from group A were oxidized in dry $O_2 + 2\%$ TCA ($C_2H_3Cl_3$) ambient at 1000 °C for 90 min and immediately annealed at the same temperature in N_2 for 30 min. The measured oxide thickness was 800 Å. After that a backside P ion implantation with a dose of 10^{16} atoms/cm² and 120 keV energy was performed through the back oxide. In order to prevent contamination, the wafers were immersed for approximately 5 s in HF to remove part of the oxide. The different wafers were annealed for different times (0, 30, 60, 90, 120 and 150 min) at 900 °C in N_2 .

Aluminium dots for MOS capacitors were deposited through a metal mask on the top oxide. The backside oxide was striped and aluminium was evaporated to make a backside contact. To reduce the density of fast surface states all wafers were sintered in a N_2/H_2 ambient at 425 °C for 30 min.

After the cleaning, on the backside of the wafers from group B, 800 Å CVD oxide was deposited. After that, the wafers from group B passed the same principal process steps, and with the same process parameters, as the wafers from group A. The only difference was that P ion implantation gettering was performed just before the oxidation. The flow chart of the principal process steps for the wafers of both groups is shown in Fig. 1.

The generation lifetime, τ_g was measured by the method of Zerbst [9] and surface generation velocity, S_0 , was measured at the depleted surface, as it was proposed by Schroder *et al.* [10]. The oxide thickness was measured by an ellipsometer.

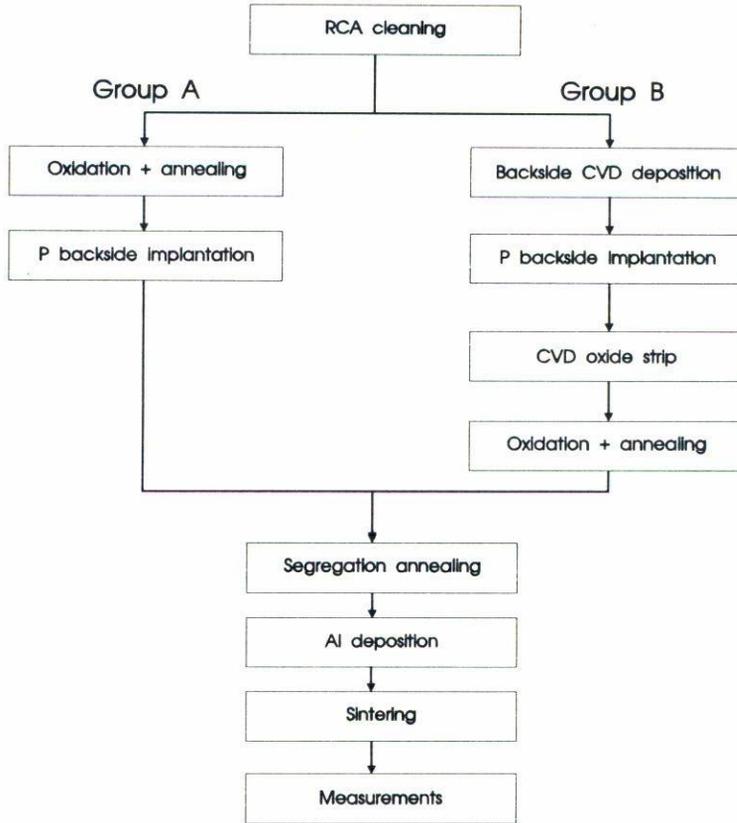


FIGURE 1. Flow chart of the principal process steps.

3. EXPERIMENTAL RESULTS AND DISCUSSION

It is known that for an efficient gettering the metallic impurities must be released from their original sites, diffuse to the gettering region and be trapped there. At a constant temperature the process of ion implantation gettering will depend on the annealing time.

As it is shown in Fig. 2, the generation lifetime in the samples of group A and B initially increases with the annealing time up to about 90 min. This means that as the annealing proceeds the metallic impurities gradually move toward the damaged region at the backside of the wafers.

For annealing times greater than 90 min the generation lifetime in the wafers of both groups decreases. There are two processes that can be responsible for the deterioration of generation lifetime in this case. First, for a long annealing time the damage created by the ion implantation can start to be annealed [11,12]. The driving force for the gettering of metallic impurities is decreased in the damaged region and the metal impurity concentration gradient causes impurities to diffuse back to the silicon bulk. Second, the degradation of the generation lifetime for anneals greater than 90 min can also be due

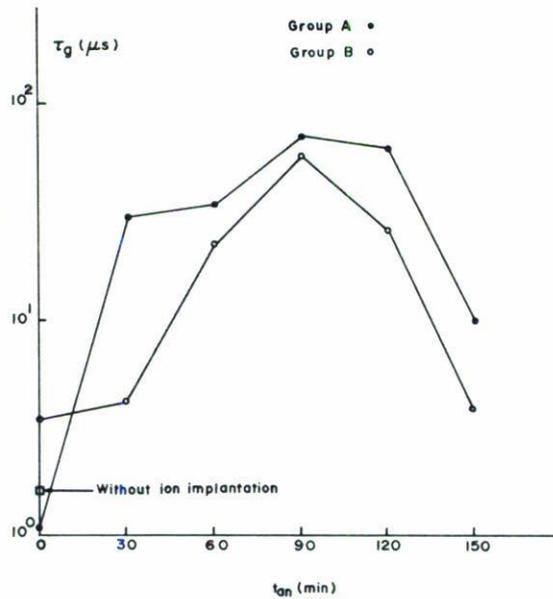


FIGURE 2. Generation lifetime as a function of annealing time in the samples of groups A and B.

to a metallic contamination from the furnace [13]. We believe that at our experimental conditions, both processes contribute to deterioration of the generation lifetime for long annealing time.

The most important fact in the present case is that the gettering performed after the oxidation (samples from group A) is more efficient than the gettering performed before oxidation (samples from group B). We suppose that this lies in the fact that during the ion implantation, the wafers with bare top surface (group B), are more easily contaminated with metallic impurities. It is well known that ion implantation contaminates wafers with metallic impurities and this contamination is dose dependent [14]. This also explains the higher surface generation velocity in the samples of group B compared to the one of group A, as can be seen in Fig. 3. From the same figure, it can be concluded that metallic impurities, as well as the gettering, affect the interface properties of MOS devices.

However, the results corresponding to zero annealing time, presented in Figs. 2 and 3, contradict the conclusions given above and need to be explained. For zero annealing time the lowest generation lifetime is in the samples of group A. The highest generation lifetime corresponds to the samples of group B, while this one in the samples without gettering has intermediate value. The highest value of the generation lifetime in the samples of group B can be explained with the effect of oxidation, which followed immediately after the implantation (see Fig. 1). The oxidation supplied the thermal energy necessary for the release and diffusion of the metallic impurities toward the backside damaged region, *i.e.*, it performed the role of segregation annealing. It is interesting to note that in spite of the

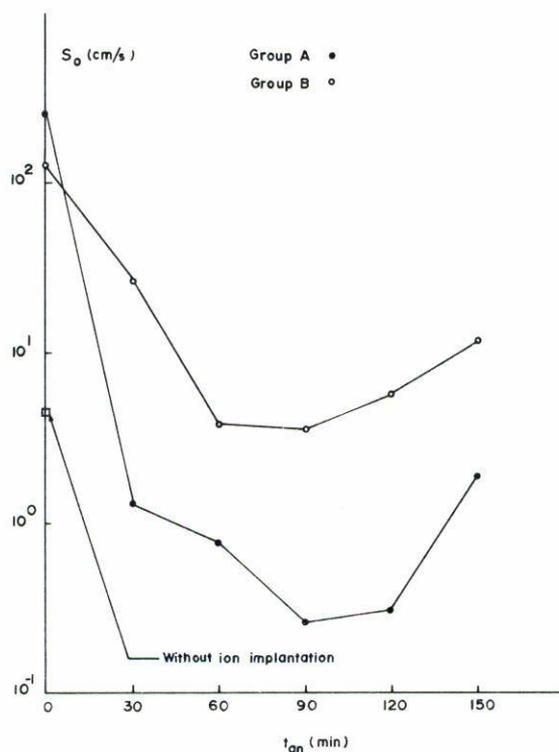


FIGURE 3. Surface generation velocity as a function of annealing time in the samples of groups A and B.

fact that the oxidation time was 90 min, the generation lifetime is much lower than this one for 90 min anneal in N_2 (see Fig. 2). This is in accordance with the segregation [15] and segregation-extended defect [16] models of the gettering. These models are based on the existence of a segregation coefficient of heavy metals between the gettering site and the silicon matrix. According to these models the segregation temperature should be as low as possible for high segregation coefficient. On the other hand the segregation annealing temperature should be sufficiently high for the release and diffusion of the metallic impurities toward the backside damaged region.

Clearly there exists an optimum annealing temperature for an efficient gettering. It has been shown that the optimum annealing temperature for the ion implantation gettering is approximately 900 °C [17]. Thus, evidently the oxidation at 1000 °C for 90 min will be less efficient as a post implantation annealing compared with the 90 min anneal at 900 °C in N_2 .

It is also evident that for a given temperature and experimental conditions, there exists an optimum annealing time. According to the segregation-extended defect model of gettering [17] for longer annealing time the damaged region can be annealed. In our case, according to Figs. 2 and 3, the optimum annealing time is 90 min.

The lowest value of the generation lifetime in the samples without annealing in group A is due to the fact that in this case there was not a supply of thermal energy necessary for the impurities to be released and diffuse to the damaged region.

The same considerations can be applied to explain the results for zero annealing time presented in Fig. 3.

Gettering experiments using isothermal segregation annealing offer the possibility to get some idea about the type of impurities.

Looking at Fig. 2, it can be seen that the τ_g vs. t_{an} curve for the samples of group A, after 30 min anneal, changes notably its slope. It could be supposed that one type of fast diffusing impurities determines the slope of this part of the curve. If it is assumed that approximately 30 min annealing is necessary for this type of impurity to be gettered, it is possible to calculate its diffusion coefficient using the relation

$$D = \frac{d^2}{t_{an}}$$

where D is the impurity diffusion coefficient, d is the wafer thickness and t_{an} is the annealing time. For $d = 300 \mu\text{m}$ and $t_{an} = 30 \text{ min}$ we obtained $D = 5.00 \times 10^{-7} \text{ cm}^2/\text{s}$. The slope of the τ_g vs. t_{an} dependence among 30 and 90 min has smaller slope. It can be supposed that another type of impurity with slower diffusivity is responsible for the change of the slope. Performing the calculations for this case, we obtained $D = 1.7 \times 10^{-7} \text{ cm}^2/\text{s}$.

Diffusion coefficients of some fast diffusers in silicon as a function of temperature are presented in Figs. 4 and 5 [18]. In the case of gold, experimentally, much of the reported data has followed one of the three lower curves (Fig. 5). Curve I corresponds to interstitial-substitution diffusion with unlimited vacancy supply through dislocations and curve II corresponds to vacancy-limited interstitial-substitution diffusion mechanism.

Some of these impurities introduce deep energy levels in the Si band gap and affect carrier lifetime [19].

Comparing experimentally determined diffusion coefficients with these ones from Figs. 4 and 5 at 900 °C, Cr and Au (curve I, Fig. 5) can be identified as the impurities that affect the generation lifetime.

A source of the Cr contamination is normally the metallic parts of the implanter [13], while Au very often exists in the starting material.

The same analysis can be performed for the τ_g vs. t_{an} curve corresponding to the wafers of group B, but taking into account the difference in the process sequence.

4. CONCLUSIONS

It has been shown that the ion implantation can introduce contamination that affects generation lifetime and surface generation velocity. The effect of this contamination is more pronounced when the implantation is performed before the oxidation. The subsequent gettering can not eliminate totally the effect of this contamination.

A simple method to identify the impurities involved in the ion implantation gettering and responsible for the improvement of generation lifetime is proposed. Cr and Au were identified as principal impurities gettered.

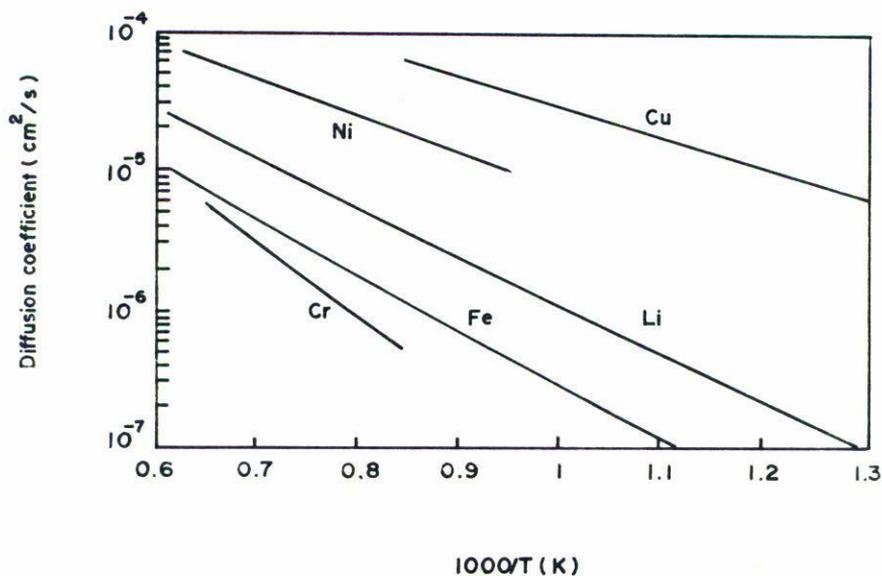


FIGURE 4. Diffusion coefficients of some fast diffusers in silicon.

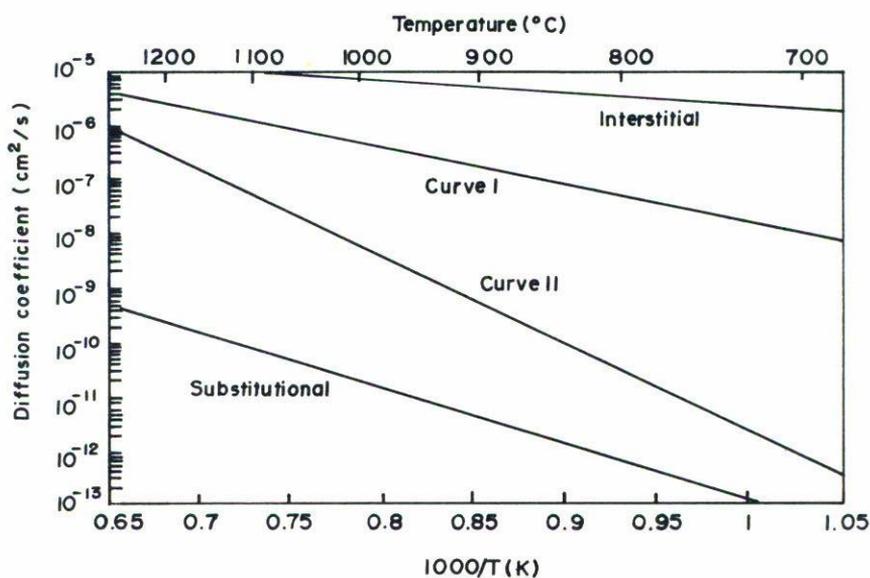


FIGURE 5. Diffusion coefficients of gold in silicon.

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REFERENCES

1. M.J. Camenzind and M.K. Balazs, *Semiconductor Silicon* (September, 1992) 89.
2. D. de Busk and J. Van Wagoner, *Semiconductor Silicon* (May, 1992) 124.
3. L. Jastrzebski, R. Soydan, H. Elabd, W. Henry and W. Savoye, *J. Electrochem. Soc.* **137** (1990) 242.
4. K. Beyer and T. Yeh, *J. Electrochem. Soc.* **129** (1982) 2527.
5. M. Nakamura, T. Kato and N. Oi, *Jap. J. Appl. Phys.* **7** (1968) 512.
6. R. Meek, T. Seidel and A. Gullis, *J. Electrochem. Soc.* **122** (1975) 786.
7. T. Buck, K. Pickar, J. Poate and C. Hsieh, *Appl. Phys. Lett.* **21** (1972) 485.
8. K. Eisele and E. Klausmann, *Solid State Technol.* (October, 1984) 177.
9. M. Zerbst, *Z. Angew. Phys.* **22** (1966) 30.
10. D.K. Schroder and J. Guldberg, *Solid State Electron.* **14** (1971) 1285.
11. A. Gullis, T. Seidel and R. Meek, *J. Appl. Phys.* **49** (1978) 5188.
12. M. Lo, J. Skalnik and P. Ordnung, *J. Electrochem. Soc.* **128** (1981) 1569.
13. L. Manchanda, J. Vasi and A.B. Bhattacharyya, *Solid-State Electron.* **23** (1980) 1015.
14. E.W. Haas, H. Glawischnig, G. Lichti and A. Bleier, *J. Electronic Mat.* **7** (1978) 525.
15. L. Baldi, G.F. Cerofolini, G. Ferla and G. Frigerio, *Phys. Stat. Solidi A* **48** (1987) 523.
16. J.S. Kang and D.K. Schroder, *J. Appl. Phys.* **65** (1989) 2974.
17. S.S. Gong and D.K. Schroder, *Solid State Electron.* **30** (1987) 209.
18. W.R. Runyan and K.E. Bean, *Semiconductor Integrated Circuit Processing Technology*, Addison-Wesley (1990).
19. A.G. Milnes, *Deep impurities in semiconductors*, John Wiley & Sons (1973).