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Investigation of Metal Oxide Semiconductor structures containing discrete interface traps

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ABSTRACT. Non-equilibrium C-V characteristics of Metal Oxide Semiconductor (MOS) structures with thermally grown SiO_2, exhibiting plateau region, were investigated. It has been shown that discrete surface traps are responsible for the plateau. The parameters of the traps were determined.

RESUMEN. En este trabajo, se investigaron capacitores MOS con óxido crecido termicamente, los cuales muestran una "meseta" en sus características C-V de no-equilibrio. Se mostró que existen trampas discretas en la interface Si–SiO_2, que son las responsables de esta meseta. Así también, se determinaron los parámetros que caracterizan a dichas trampas.

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1. INTRODUCTION

Simmons and Wei [1] developed the theory of dynamic characteristics of Metal Oxide Semiconductor (MOS) capacitors containing discrete interface traps. They have shown that when the interface traps are in dynamic equilibrium with the voltage ramp, the device exhibits steady-state charge and capacitance characteristics. When the interface traps are out of equilibrium with the voltage ramp, then the emission of trapped charge is a function of the time only and not of the voltage. Under such conditions, the characteristics are considered to be non steady-state in nature. The emission of trapped charge in non steady-state gives rise to a plateau (ledge) in the C-V characteristics. The transition from steady-state to the non-equilibrium state results in kinks in the C-V characteristics.

To the best of our knowledge there are no reported experimental results which demonstrate the effects of discrete interface traps in MOS structures with thermally grown SiO_2, described by the theory of Wei and Simmons [2]. In the present work experimental results, which demonstrate the existance of discrete interface traps in MOS structures with thermally grown oxide, are presented. The influence of these traps on the non-equilibrium C-V curves is demonstrated. An analisis of the experimental results, on the basis of the theory of Simmons and Wei, is performed and the parameters of the traps are determined.

2. Samples preparation and measurements

MOS capacitors were fabricated on n-type 2–5 Ω cm, (100) oriented, CZ grown Si wafers. The wafers were cleaned by the standard RCA process. The oxidation was performed at 1000 °C in dry O_2 + 2% TCA ($C_2H_3Cl_3$) for 90 min. The wafers were annealed at the same temperature in N_2 for 30 min. The measured oxide thickness was 800 Å. After that, a backside P implantation with a dose of 10^{16} atoms/cm^3 and 120 KeV energy was performed. The wafers were annealed at 900 °C in N_2 for 60 min. Part of the oxide was etched to prevent the contamination due to the ion implantation. The final oxide, measured by an ellipsometer, was 449 Å. The backside oxide was striped. Aluminum dots for MOS capacitors were deposited through a metal mask on the top oxide. On the backside of the wafers aluminum was also evaporated and the wafers were sintered in a N_2/H_2 ambient at 425 °C for 30 min. The sine-voltage C-V method [3] was used in this experiment. The h.f. (high frequency) C-V curves were measured with Boonton 72B capacitance meter at 1 MHz. Wavetek model 271 function generator was used as a sine-voltage source.

3. Experimental results and discussion

During the measurements some MOS capacitors have shown anomalous non-equilibrium sine-voltage C-V curves. In Fig. 1, a typical family of anomalous C-V curves for one of the capacitors is presented. The different curves correspond to different voltage sweep rates $R = dV/dt = V_0 + V_a\omega cos(\omega t)$, where V_0 is the initial voltage, V_a is the voltage amplitude, ω is the angular frequency and t is the time. In this particular case the voltage amplitud was kept constant and R was changing by changing the frequency. As can be seen from Fig. 1 the C-V curves exhibit a plateau which decreases and finally desapears with the increase of the sweeping rate R. According to the theory of Simmons and Wei [1], such an effect can be observed when discrete traps exist at the insulator-semiconductor interface. Now, we shall try to explain the anomalous behavior of the present experimental C-V curves on the basis of this theory.

When the sweep rate is very low the MOS capacitor is in dynamic equilibrium with the voltage ramp at all times and the C-V curve does not exhibit hysteresis (Fig. 2). However, as can be seen from Fig. 1 the increase of the voltage sweep rate produces a hysteresis on the C-V curves for negative voltage sweep cycles. Moreover, the C-V curves exhibit plateau, which disapears with the increase of the voltage sweeping rate. This effect can not be explained on the basis of the bulk generation alone, as can be demonstrated.

With the application of a negative going voltage ramp (n-type substrate, $V_0 = 0$) the width of the depletion region continues to grow until such times that the rate of increase of the charge, associated with the arrival of holes (generated in the depletion region) at the Si–SiO_2 interface, is just sufficient to balance the rate of increase of charge on the gate. Thus, when the depletion region reachs its maximum any further increase in the gate voltage is dropped across the insulator, so the gate charge, Q_g, increases with $C_{ox}|dV/dt|$.

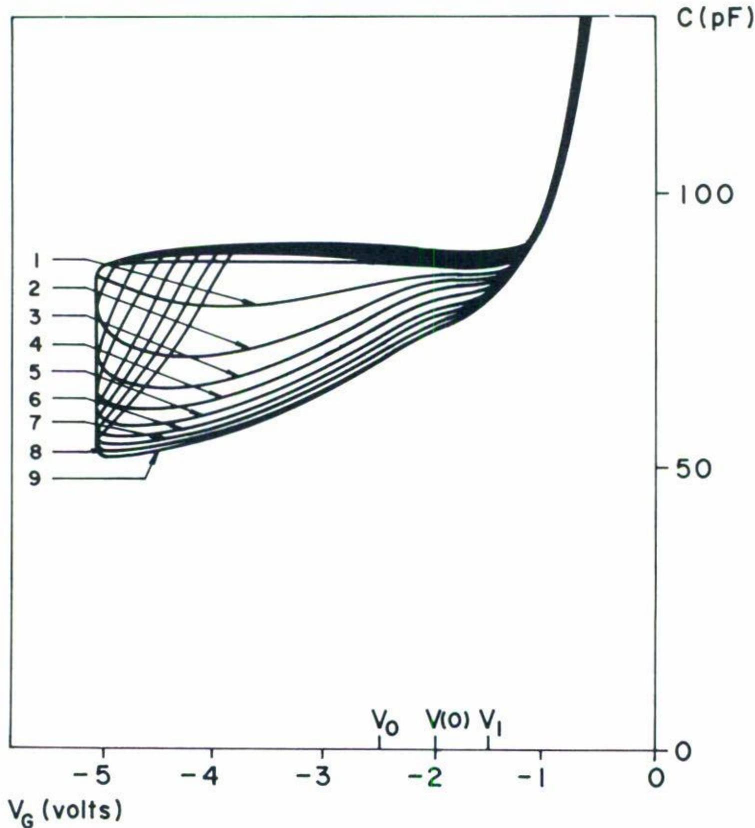

FIGURE 1. Experimental C-V curves with $V_a = -5$ V and sweep frequency of 10, 20, 30, 40, 50, 60, 70, 80 and 90 mHz for the curves 1, 2, 3, 4, 5, 6, 7, 8 and 9, respectively.

If the bulk generation alone is responsible, then, at the capacitance of the plateau we have

$$qGW_{\max} = C_{\text{ox}} \left| \frac{dV}{dt} \right| = RC_{\text{ox}}, \tag{1}$$

where G is the generation rate in the semiconductor depletion region, C_{ox} is the oxide capacitance, $W_{\max}$ is the maximum depletion layer width and q is the electron charge. However, Eq. (1) predicts that for given combination of V_a and ω the depletion region width reachs a maximum for $R_{\max}$ and hence that the capacitance reachs a minimum rather than reachs a relative minimum (the plateau), and then decreases again. This means that in order for the capacitance to exhibit a plateau, there must be an additional source of holes that keeps the depletion region width almost a constant, before reaching its maximum. The reason for the observed phenomenon lies in the fact that large density of traps exist at the Si–SiO_2 interface. Surface generation of electron-hole pairs occurs through these traps, which process take place at a very low rate initially due to the surface generation centers being filled with electrons. As these generation centers empty their electrons, more efficient generation of carriers take place and the surface generation current increases with the time. It may exceed the displacement current $C_{\text{ox}}|dV/dt|$, provided that the sweep

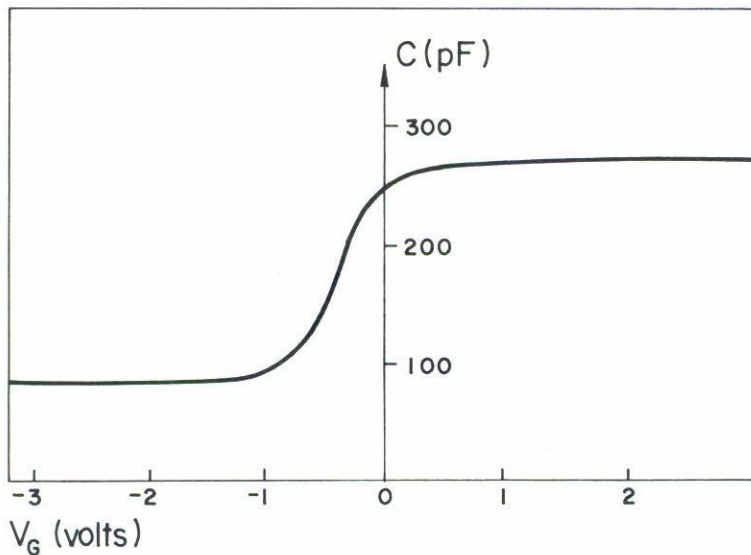

FIGURE 2. Experimental h.f. curve of the capacitor of Fig. 1 with sweeping frequency of 4 mHz.

rate is low enough to allow the generation process take place and high enough to keep the device in non-steady state. This non-steady state process provides extra positive charge to the surface, thereby keeping the depletion region width almost a constant, which explains the plateau region on the C-V curves for negative voltage cycles. At a later time, surface generation current decreases rapidly, when free holes are gathered at the surface, causing again inefficient generation.

Now, we shall analyze our experimental results (Figs. 1 and 2) and try to determine the parameters of the traps using the theory of Simmons and Wei [1]. If the trap level is below the equilibrium Fermi level, then at flat band condition the traps are filled and the flat band voltage is given by

$$V_{\text{fb}} = -\frac{Q_{\text{ox}}}{C_{\text{ox}}} - \frac{Q_{\text{t}}}{C_{\text{ox}}} + \phi_{\text{ms}}, \tag{2}$$

with the trapped charge given by $Q_{\text{t}} = -qN_{\text{t}}$, where Q_{ox} is the oxide charge and ϕ_{ms} is the metal-semiconductor work function difference. As the voltage decreases, the capacitance decreases according to

$$\frac{C}{C_{\text{ox}}} = \left[1 - \frac{2C_{\text{ox}}^2}{qN_D K_{\text{s}}\epsilon_0}\left(\frac{Q_{\text{ox}} + Q_{\text{t}}}{C_{\text{ox}}} - \phi_{\text{ms}} + V\right)\right]^{-1/2}, \tag{3}$$

where N_D is the impurity concentration, K_{s} is the dielectric constant of the semiconductor and ϵ_0 is the free space permittivity. When the surface potential reachs a value given by

$$q\psi_{\text{s}} = E_{\text{F}} - E_{\text{t}}, \tag{4}$$

where $E_{\rm t}$ is the trap energy level and $E_{\rm F}$ is the Fermi level, then V is given by V_1 (Fig. 1, curve 1),

$$V_1 = \frac{qN_{\rm t}}{C_{\rm ox}} - \frac{\sqrt{2qN_D\epsilon_0 K_{\rm s}(E_{\rm F}-E_{\rm t})}}{C_{\rm ox}} - \frac{Q_{\rm ox}}{C_{\rm ox}} - E_{\rm F} + E_{\rm t} + \phi_{\rm ms}, \tag{5}$$

and the electrons start to escape from the surface. Taking into account that plateau capacitance, $C_{\rm t}$, is equal to the equilibrium inversion capacitance, $C_{\rm F}$, one can assumes that in this case the traps are in dynamic equilibrium with the semiconductor conduction band. Thus, further decrease in the gate voltage results in release of electrons from the interface traps to the conduction band, rather than the depletion region growing in size, in order that

$$Q_{\rm g} + Q_{\rm D} + Q_{\rm ox} + Q_{\rm t} = 0 \tag{6}$$

will be satisfaced, and where $Q_{\rm D}$ is the semiconductor depletion charge and $Q_{\rm g}$ is the charge on the gate. The surface potential $\psi_{\rm s}$, is therefore "pinned" to the value given by Eq. (4) until such times as the traps are completly empty. Thus, the capacitance is independent of V, and the traps are in dynamic equilibrium with the conduction band. Then according to [1] we can write

$$\frac{C}{C_{\rm ox}} = \left[C_{\rm ox}\sqrt{\frac{2(2E_{\rm F}-E_{\rm t})}{qN_D\epsilon_0 K_{\rm s}}}\right]^{-1}. \tag{7}$$

At point $V = V_0$ (curve 1, Fig. 1) the traps are empty and the capacitor goes into deep depletion mode in order to maintain charge balance Eq. (6). For $V < V_0$, the capacitance is given by Eq. (3) but with $Q_{\rm t} = 0$.

Now we consider the case when the voltage sweep rate is increasead and at some particular voltage $V(0)$ the traps can not emit charge at the rate the charge is changing at the gate, that is

$$\left|\frac{dQ_{\rm g}}{dt}\right| > \left|\frac{dQ_{\rm t}}{dt}\right|, \tag{8}$$

the traps are in non-equilibrium with the conduction band and the device goes into a deep depletion mode (Fig. 1, the point on the curve 2, corresponding to $V = V(0)$). In this case, the capacitance is given by Eq. (3), but with $Q_{\rm t}$ as a function of time. In the non-steady state, if the trap level is more than a few kT above the equilibrium Fermi level, the rate of change in the surface traps is given by

$$\frac{dQ_{\rm t}}{dt} = -e_n Q_{\rm t}, \tag{9}$$

where e_n is the emission probability, given by

$$e_n = \nu\sigma_n N_{\rm c}\exp\left(\frac{E_{\rm g}-E_{\rm t}}{kT}\right), \tag{10}$$

TABLE I. Basic parameters of the MOS capacitor from Figs. 1 and 2.

C_{ox} (pF)	C_F (pF)	C_t (pF)	$A \times 10^{-3}$ (cm^2)	d_{ox} (Å)	$N_D \times 10^{16}$ (cm^3)	ϕ_{ms} (V)	V_1 (V)	$V(0)$ (V)	R_1 (V/s)	V_{fb} (V)
270	85	85	3.51	449	1.0	−0.237	−1.5	−2.0	0.156	−0.25

TABLE II. Parameters used in the calculations.

u_b	ϕ_b (V)	$\nu \times 10^7$ (cm/s)	$N_c \times 10^{19}$ (cm^{-3})	$n_i \times 10^{10}$ (cm^{-3})	K_s	$\epsilon_0 \times 10^{-14}$ (F/cm)	K_{ox}	E_g (eV)	T (°C)
13.72	0.352	2.5	3.16	1.11	11.9	8.85	3.9	1.12	24

where ν is the thermal velocity, σ_n is the electron capture cross section, N_c is the effective density of states in the conduction band and E_g is the band gap. Integrating Eq. (9) we obtain the trapped charge as a function of time:

$$Q_t(t) = Q_t(0, V(0)) \exp(-e_n t), \tag{11}$$

where t is the time, $V(0)$ is the gate voltage and $Q_t(0, V(0))$ is the charge at the instant when the capacitor goes into the non-steady state. According to [1], in this case we can write

$$V(0) = \frac{R}{e_n} - \frac{\sqrt{2qN_D\epsilon_0 K_s(E_F - E_t)}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}} - E_F + E_t + \phi_{ms}. \tag{12}$$

Using the experimental results from Figs. 1 and 2, the basic parameters of the MOS capacitor were calculated and are presented in Table I, where d_{ox} is the oxide thickness and $R = R_1$ is the voltage sweep rate at $V = V(0)$ (curve 2, Fig. 1). In Table II the rest of the parameters which have been used in the calculations are presented, where u_b is the bulk dimentionless potential, ϕ_b is the bulk potential, n_i is the intrinsic carrier concentration and K_{ox} is the dielectric constant of the oxide.

Using Eq. (4) and the data from Tables I and II we obtain

$$E_F - E_t = 0.674 \text{ eV}.$$

To determine trap density N_t first of all we have to determine oxide charge density Q_{ox}. For the purpose we substitute in Eq. (5) the value of $E_F - E_t$ and replace V_1 with V_0 (curve 1, Fig. 1), where $Q_t = 0$. By this way we obtained $Q_{ox} = 7.46 \times 10^{-8}$ coul/cm^2. Now, substituting the value of Q_{ox} in Eq. (5) we calculated the density of the traps in the point on the curve 1 corresponding to $V = V_1$, where they are filled with electrons. Thus, we obtained $N_t = 4.81 \times 10^{11}$ cm^{-2}.

Applying Eq. (12) for the point of the C-V curve corresponding to $V = V(0)$ (curve 2, Fig. 1), we obtained $e_n = 3.1 \times 10^{-1}$ s. The obtained value of the emission constant permited us to make an atempt to determine trap capture cross-section σ_n. The relation

between the electron emission constant and the electron capture cross-section of the trap is given by

$$\sigma_n = \frac{e_n}{\nu N_c} \exp\left(\frac{E_g - E_t}{kT}\right), \tag{13}$$

with

$$N_c = 5.46 \times 10^{15} T^{3/2}.$$

Substituting the corresponding values of the parameters in Eq. (13) we obtained

$$\sigma_n = 3.25 \times 10^{-13}\ \text{cm}^2$$

However, in Eq. (13) flat band condition is assumed as well as that the traps are filled up to the Fermi level. Taking into account that in reality the device is biased in the depletion mode, then $E_t = E_F - q|\psi_s|$ and using the relation $E_t = E_F = E_g - kT\ln(N_c/N_D)$, Eq. (13) becomes

$$\sigma_n = \frac{e_n}{\nu N_D} \exp\left(\frac{q|\psi_s|}{kT}\right). \tag{14}$$

Substituting the values of the corresponding parameters in Eq. (14) we obtained

$$\sigma_n = 1.27 \times 10^{-12}\ \text{cm}^2.$$

4. CONCLUSIONS

It has been experimentally demonstrated the existence of dicrete interface traps in MOS structures with thermally grown SiO_2. The influence of these discrete traps on the non-equilibrium C-V curves is in accordance with this predicted by the theory of Simmons and Wei [1]. Using this theory the parameters of the traps were determinated.

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REFERENCES

1. J.G. Simmons and L.S. Wei, *Sol. State Elec.* **16** (1973) 43.
2. L.S. Wei and J.G. Simmons, *Sol. State Elec.* **17** (1974) 1021.
3. P. Peykov, T. Diaz and J. Carrillo, *Phys. Stat. Solidi (a)* **129** (1992) 201.