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The effect of extrinsic contamination on ion implantation gettering*

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Abstract. A fast two-points MOS C-t method for measurement of carrier diffusion length, and hence recombination lifetime, is proposed. Combining generation and recombination lifetime measurements, the kinetics of impurities during the process of gettering is investigated. This approach enabled us to distinguish, in the present case, an extrinsic contamination on the wafer surface. The existence of an extrinsic contamination, in addition to the intrinsic one, introduces new variables in the gettering process that can affect gettering efficiency.

Resumen. Se propone un método rápido, MOS C-t de dos puntos, para medir la longitud de difusión y por lo tanto el tiempo de vida de recombinación de los portadores. Usando la medición combinada del tiempo de vida de generación y de recombinación, se investigó la cinética de las impurezas durante el proceso de "gettering". Este enfoque nos permitió distinguir, en el presente caso, la existencia de una contaminación extrínseca sobre la superficie de la oblea. Esta contaminación, junto con la contaminación intrínseca, introducen nuevas variables en el proceso de "gettering", las cuales pueden afectar su eficiencia.

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1. Introduction

During the IC's (integrated circuits) fabrication process, defects (different to the intrinsic defects in the wafer) can be induced. Most of the process-induced defects are due to contamination (mainly metallic impurities) originated by chemicals [1], equipment [2], ambient [3], wafer manipulation [4], etc.

Besides the efforts to prevent the wafer's contamination, techniques (such as gettering) have been developed to reduce or eliminate defects in the region where semiconductor devices are fabricated. The gettering techniques can be divided into two groups: intrinsic and extrinsic gettering. Usually intrinsic gettering is performed by a three step anneal of CZ grown Si. The first high-temperature step leads to out-diffusion of oxygen and creates a denuded zone at the surfaces. A high density of nuclei for oxygen precipitates are induced in the bulk of the wafer during the second low-temperature annealing step. The third step of the high-temperature annealing is responsible for the growth of oxygen precipitates and it is responsible for the gettering.

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In the extrinsic gettering, controlling defects are usually introduced at the backside of the wafer by one of the following techniques: ion implantation [5], diffusion [6], Si_3N_4 deposition [7], metal deposition [8], mechanical damage [9], laser damage [10], etc. These techniques produce that the defects diffuse far away from the surface of the wafer.

Although a great number of works on this matter have been published, the exact gettering mechanisms are still not well established [11]. Moreover, there are many unanswered questions concerning gettering. Some of these questions are: How efficient is the gettering in regard to impurity contamination introduced during the gettering process? How many impurities can be gettered? Is every gettering technique so efficient for all impurities? and if not, which gettering technique is efficient for a given type of impurity?, etc.

Normally, for a given gettering technique there are optimum conditions to get maximum efficiency. It is known, that for ion implantation gettering the parameters that determine the optimum gettering conditions are the ion dose and energy, and the temperature and time of the post-implantation annealing. The first two parameters determine the formation of highly defected gettering region, which serves as a sink for the impurities. The second two parameters are responsible for the thermal energy and the time necessary so that the defects (especially metallic impurities) can be released from its associated site, diffuse to the gettering region, and be captured at the gettering sites.

In the case of P ion implantation gettering we have found that the optimum gettering conditions are: ion implantation $E > 70$ KeV, with a dose of 10^{16} cm^{-2} and post-implantation annealing at $T \approx 900°C$ and $t \approx 90$ minutes. These values have been experimentally confirmed in many occasions by us and diverse authors, and they can be explained on the basis of the existing models [11]. However, other factors besides the main gettering process parameters can affect gettering efficiency. In the present work we have investigated and identified other factors, in addition to the main gettering process parameters, which affect ion implantation gettering efficiency.

MOS (metal-oxide-semiconductor) structures were used as test devices. Carrier lifetime was chosen as a measurable parameter for monitoring the gettering efficiency. The method of carrier lifetime measurement provides the most realistic analysis considering that it is more sensitive to the impurities, or other kinds of crystalline defects, than the chemical and physical trace analysis methods, and because it is directly related to device characteristics of interest [12]. Generation lifetime, τ_g, characterizes the material near the wafer surface over the width of SCR (space charge region) and the recombination lifetime, τ_r, characterizes the semiconductor's volume over a diffusion length of the minority carrier from the SCR. Measuring τ_g and τ_r permits to monitor the existence and the behavior of impurities during the gettering process in the near surface device active region of the wafer.

2. MEASUREMENT OF GENERATION AND RECOMBINATION LIFETIME

There are different methods to measure the generation lifetime [13–15], recombination lifetime [16, 17] or both in the same structure [18]. To obtain statistically reliable results is necessary to measure a large number of samples. However, in the case of carrier lifetime measurements, the improvement of material quality has resulted in large values

of carrier lifetime. For instance, for generation lifetime ≈ 3.0 ms the MOS capacitance relaxation time, t_F, is about 17 minutes [18]. This has provoked the implementation of rapid measurement techniques [19–21].

Let us first consider the theoretical basis of the measurement techniques used. When a MOS capacitor, at room temperature, is driven in deep depletion condition, by applying a depleting voltage pulse, it returns to quasi-equilibrium inversion condition as a result of bulk and surface thermal carrier generation. In this case the transient behavior of the capacitor is described by the equation [13]

$$-\frac{\epsilon_0 K_s N_D}{2C_{ox}} \frac{d}{dt}\left[\frac{C_{ox}}{C}\right]^2 = \frac{\epsilon_0 K_s n_i}{\tau_g C_F}\left(\frac{C_F}{C} - 1\right) + n_i S, \tag{1}$$

where N_D is the substrate doping concentration (n-type semiconductor), ϵ_0 is the permitivity of the free space, K_s is the dielectric constant of silicon, C_{ox} is the oxide capacitance, C_F is the final inversion capacitance, C is the capacitance, n_i is the intrinsic carrier concentration and S is the surface generation velocity.

It has been shown that good approximation of the above equation is [19]

$$\tau_g = \frac{n_i C_F}{8 N_D C_{ox}}\left(1 + \frac{C_i}{C_F}\right)^2 t_F, \tag{2}$$

where the minimal initial capacitance, after the application of the voltage pulse, at $t = 0$ is C_i.

In the case of high temperature, it is necessary to take into account the contribution of the bulk diffusion current to the capacitance relaxation. In this case Eq. (1) has the form

$$-\frac{\epsilon_s K_s N_D}{2C_{ox}} \frac{d}{dt}\left[\frac{C_{ox}}{C}\right]^2 = \frac{\epsilon_0 K_s n_i}{\tau_g C_{ox}}\left(\frac{C_F}{C} - 1\right) + n_i S + \frac{n_i^2 D_p}{L_p N_D}, \tag{3}$$

where L_p is the minority carrier diffusion length and D_p is the carrier diffusion coefficient.

At sufficiently high temperature, the third term in the right hand side of Eq. (3) is dominant. In this case, after some transformations, Eq. (3) becomes

$$-\frac{1}{C}\frac{d}{dt}\left(\frac{1}{C}\right) = \frac{n_i^2 D_p}{\epsilon_0 K_s C_{ox} N_D^2 L_p}. \tag{4}$$

Integrating from the beginning, $t = 0$, to the end, $t = t_F$, of the transient process requires integrating C, from C_i to C_F:

$$-\int_{C_i}^{C_F} \frac{1}{C}\, d\left(\frac{1}{C}\right) = \frac{n_i^2 D_p}{\epsilon_0 K_s C_{ox} N_D^2 L_p}\int_0^{t_F} dt. \tag{5}$$

As a result we obtain

$$L_p = \frac{2 n_i^2 D_p C_F^2}{\epsilon_0 K_s N_D^2 C_{ox}}\left(\frac{C_F^2}{C_i^2} - 1\right)^{-1} t_F. \tag{6}$$

The intrinsic carrier concentration is given by the expression [22]

$$n_i = 3.87 \times 10^{16} T^{1.5} \exp(-0.605/kT), \tag{7}$$

where k is the Boltzman's constant and T is the temperature. The hole diffusion constant is calculated from the expression

$$D_p = 12.8\,(300/T)^{1.2}. \tag{8}$$

Using Eqs. (6), (7) and (8) and the measured values of N_D, C_{ox}, C_F, C_i and t_F recombination lifetime,

$$\tau_r = \frac{L_p^2}{D_p}, \tag{9}$$

can be obtained.

3. Samples preparation

MOS capacitors for this experiment were fabricated in n–type, (100) oriented, CZ grown, 2–5 ohm-cm Si wafers. Several lots of wafers were cleaned by the standard RCA process. The oxidation was performed at 1000°C in dry O_2 + 2% TCA ($C_2H_3Cl_3$) ambient. The oxide thickness, measured by an ellipsometer, was 800 Å. After the oxidation a thermal treatment in ambient of N_2 at 1000°C during 30 minutes was performed. The wafers were gettered by a backside P ion implantation with the optimum parameters E = 120 KeV and $D = 10^{16}$ cm^{-2}. Different wafers were annealed at the optimum temperature of 900°C in N_2 for different times (0, 30, 60, 90, 120 and 150 minutes). High purity aluminum gate electrodes were evaporated on the top oxide through a metal mask. On the backside of the wafers, after oxide striping, aluminum was also evaporated. All wafers were annealed in N_2/H_2 ambient at 425°C for 30 minutes.

4. Measurements

MOS C-t measurements were performed at room temperature and the generation lifetime was calculated using Eq. (2). To obtain the minority carrier diffusion length [Eq. (6)] and hence the recombination lifetime, C-t measurements at different temperatures were performed. All the C-t measurements were performed with a PAR capacitance meter and the temperature was controlled with Temptronic model TP36 Termochuck System with accuracy ±1°C.

In the case of $L_p(\tau_r)$ measurements it is very important to know the breakpoint temperature, *i.e.*, the temperature in which Eq. (4) begin to be valid. An easy way to find the breakpoint temperature is to plot t_F *vs.* $1/T$. It has been shown [19] that the slope of this plot, at near room temperature, is approximately proportional to n_i^{-1} and at elevated

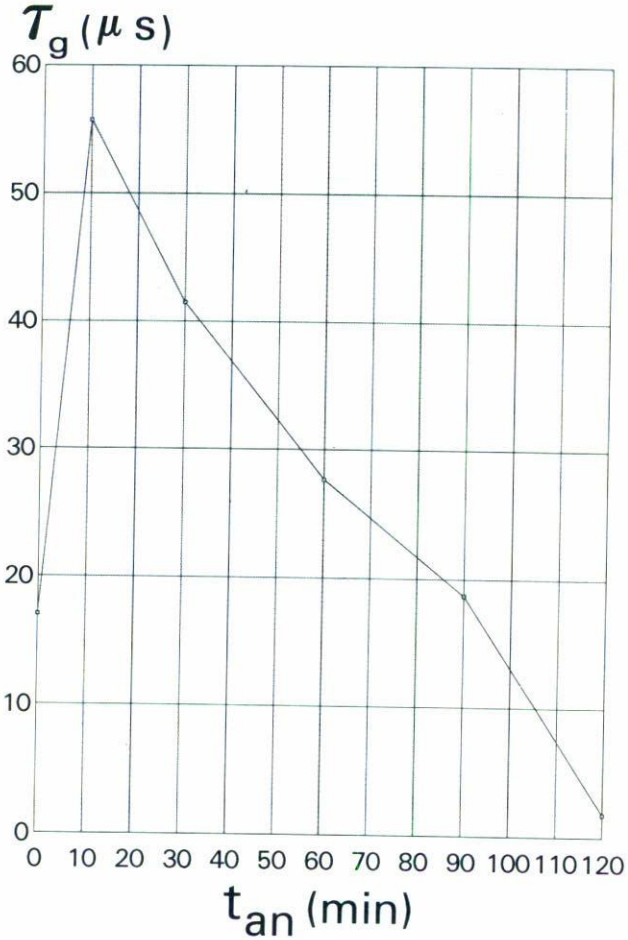

FIGURE 1. Generation lifetime *vs.* annealing time.

temperatures it is proportional to n_i^{-2}. The temperature at which the slope change is the breakpoint temperature.

5. EXPERIMENTAL RESULTS AND DISCUSSION

In all wafer lots, the generation lifetime was measured, and they have the same behavior as a function of post-implantation annealing time, t_{an}, but lot A was an exception. The general behavior as a function of t_{an} coincides with our previous results, *i.e.*, the maximum gettering efficiency was found at 90 minutes annealing, with generation lifetime $\approx$ 75 ms. However, in lot A, generation lifetime showed different peculiar behavior and different values as a function of t_{an}. In this case, the maximum τ_g was found at 10 minutes as shown in the τ_g *vs.* t_{an} plot of Fig. 1. This shows that for annealing time greater than 10 minutes, the generation lifetime (or gettering efficiency) deteriorates rapidly. To explain

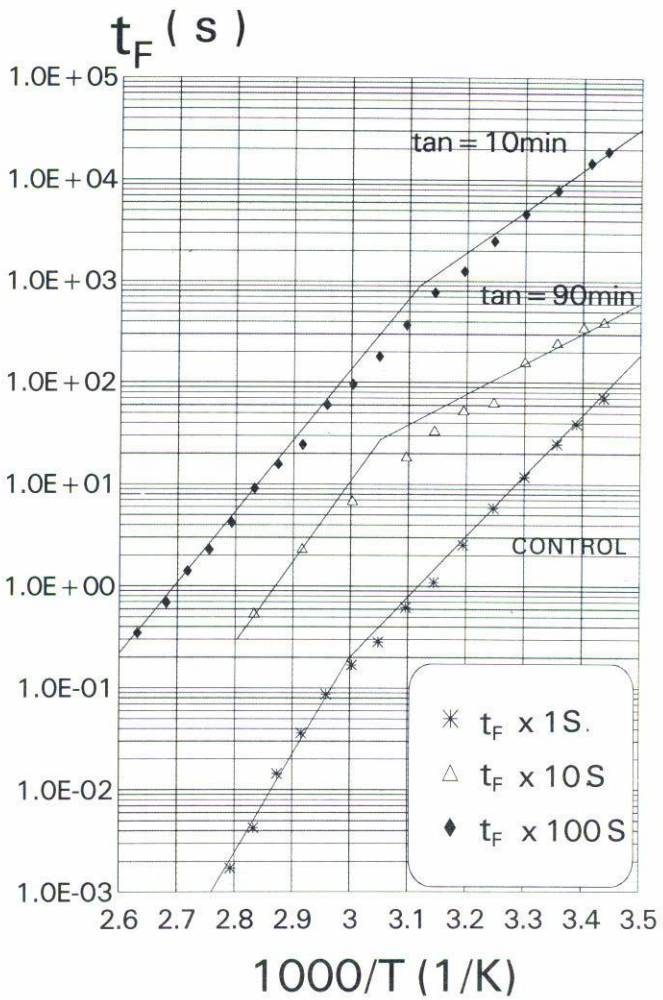

FIGURE 2. Capacitance relaxation time *vs.* temperature.

this behavior of τ_g as well as to better understand how the gettering process proceeds, we measured the minority carrier diffusion length and calculated τ_r by the method proposed above. Figure 2 is the t_F *vs.* $1/T$ for three typical samples of lot A. The slope change of these plots demonstrates clearly the breakpoint temperature, T_{BR}, for every sample. For temperatures higher than T_{BR} the quasi-neutral bulk generation (diffusion current) is dominant, while for lower temperatures the space-charge thermal generation (generation current) is dominant. Between these two regions, one can see the transition region, where both mechanisms contribute to the capacitance relaxation. According to Fig. 2, the breakpoint temperatures for the samples without gettering (*), with gettering and annealed for 10 minutes (♦) and 90 minutes (△) are 61.7, 48.2 and 55.1°C, respectively. Comparing these results with the results in Fig. 1, it is possible to see that the lower breakpoint temperature corresponds to the samples with higher generation lifetime, in agreement with the theory.

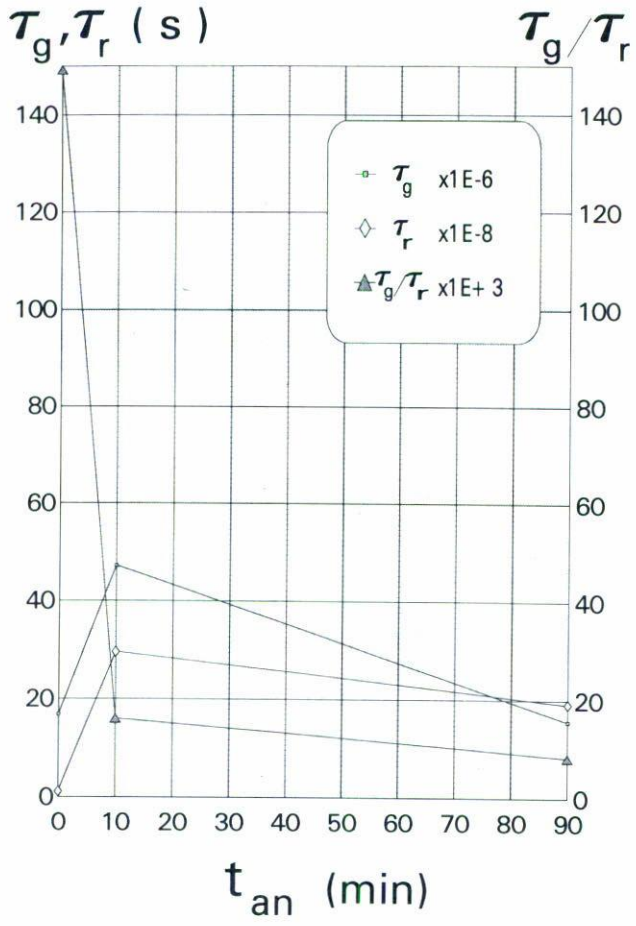

FIGURE 3. Generation lifetime, recombination lifetime and the ratio generation lifetime/recombination lifetime *vs.* annealing time.

The minority carrier recombination lifetime was calculated from C-t measurements at higher temperatures than T_{BR}. Using the highest temperatures we assure that the capacitance relaxation is governed only by the quasi-neutral bulk generation. In the Fig. 3 the plots of τ_r, τ_g and τ_g/τ_r *vs.* t_{an}, for these 3 samples, is presented (the corresponding values of τ_g are these ones of Fig. 1). In this figure, we can see that the recombination lifetime follows the behavior of generation lifetime. Its maximum is at 10 minutes anneal and after that decreases. However, τ_g/τ_r *vs.* t_{an} plot is the most interesting. This ratio decreases with t_{an} for all annealing times. As was mentioned above, τ_g characterizes the SCR and τ_r characterizes the region below the SCR, then, we can conclude, that some impurities penetrate from the semiconductor surface into the bulk affecting first τ_g and after that τ_r. We can conclude, also, than the diffusion of the impurities is faster than the velocity of gettering.

One can think that exist two impurities flows. The first one consists of impurities which are gettered at the backside of the wafer, and the second one consists of extrinsic impurities which penetrate from the wafer surface. For short annealing times (10 minutes) the wafer

bulk is cleaned of impurities to some degree, due to the gettering effect. However, soon this process is dominated by the impurity diffusion from the contaminated surface, if the surface is contaminated. Base on this supposition, one can suppose that during the wafer processing and/or wafer handling the surface of lot A was contaminated.

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