Revista Mexicana de Física **42**, *No. 3 (1996) 459–466*

OTA-GS filters: the new face of RC-active filters

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Recibido el 12 de julio de 1995; aceptado el 7 de diciembre de 1995

ABSTRACT. An approach for the direct translation of conventional RC active filters into CMOS integrable structures is presented. This technique is based on the replacement of resistors by differential gain stages, and of op-amps by single ended gain stages. A high-frequency compensated CMOS universal filter derived using this method is shown and experimentally verified.

RESUMEN. Se presenta un enfoque para transformar directamente estructuras de filtros activos RC convencionales a estructuras CMOS integrables. Esta técnica se basa en la substitución de resistencias por etapas de ganancia diferencial y de amplificadores operacionales por etapas de ganancia con entrada referida a tierra. Se muestra la derivación de un filtro universal compensado de alta frecuencia utilizando este método. Se muestran también resultados experimentales que verifican este filtro.

PACS: 07.50.Ek; 07.50.Qx; 07.50.Yd

1. INTRODUCTION

RC active filters which use resistors, capacitors, and op-amps were initially implemented, either, with discrete components or as hybrid microcircuits in thin-or thick-film technology. RC active filters was a very prolific area of research during the sixties and seventies. During this period, many RC active filter structures were reported. They were finally classified into families with well understood characteristics regarding active and passive sensitivities, component spread, number of op-amps, and as some other design trade-offs [1, 2]. In the eighties, the drive for integration lead to the translation of RC active filters into MOSFET-C circuits. In the case of MOSFET-C filters, resistors were simulated using MOS transitors in ohmic mode [3,4]. This approach presents several problems: 1) It requires long MOS transistors with large parasitic capacitances. These capacitances introduce relatively low-frequency poles; at least one for each simulated resistor. The excess phase of these poles and of the op-amps makes implementation of high frequency and/or highly selective filters very difficult. 2) Long MOS transistors behave, in practice, as RC distributed lines rather than as purely resistive elements [5]. Filter design, taking this into account, can become very involved. 3) Dynamic range and tuning range are severely limited in order to keep transitors in ohmic mode. 4) Op-amps with output stages are required in the MOSFET-C approach. The reason for this, being that the op-amps must

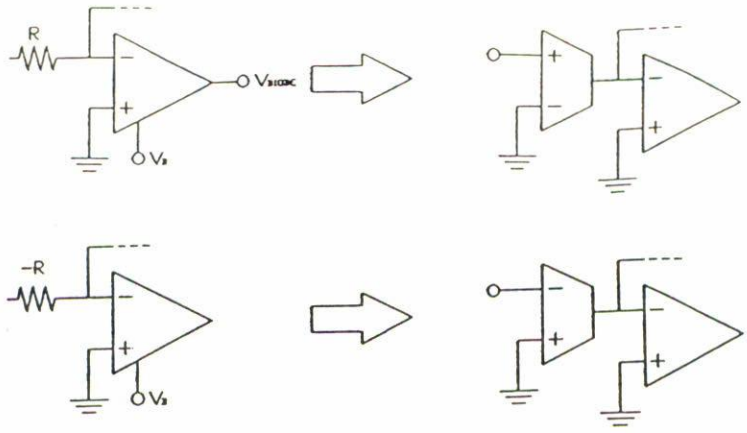

FIGURE 1. (a) Positive R op-amp section and OTA-implementation; (b) negative R op-amp section and OTA implementation

drive resistive loads. The driver-stage further limits the maximum frequency of operation in the MOSFET-C approach. In this paper, we show an alternative approach to directly translate RC active filter structures into compact integratable CMOS circuits with very good high-frequency characteristics. The method is described in Sec. 2 of this paper. Section 3 introduces a universal filter derived from this technique. Section 4 shows simulations of a CMOS universal filter currently in fabrication; and it also shows experimental results from of a breadboard prototype. Section 5 provides conclusions.

2. OTA-GS FILTERS DERIVED FROM RC ACTIVE FILTERS

2.1. Resistor simulation

The proposed approach is based on replacing the resistors in the RC active prototype by transductors (OTAs) which, in their simplest form, are gain stages or differential amplifiers with active loads (see Fig. 1). The transconductance gain (g_{mR}) of the transconductor is reciprocal to the value of the simulated resistance: $R = 1/g_{mR}$. The approach follows a similar line to that proposed by Refs. [6] and [7]. The main advantages are: 1) The requirements on the transductor are relaxed: specifically, high output impedance and high output signal swing are not required from the OTA since its output node is connected to a virtual ground (the input of the op-amp). 2) Because of this reason, transductors can be implemented by using very simple structures such as gain stages, differential pairs, actively loaded differential pairs, etc. (Fig. 2). In all cases, a simple transconductor has only very high frequency parasitic poles. In order to obtain a linear transconductor with wide tuning range, the differential pair can be replaced by a very compact six-transistor cell reported by the author in Ref. [8]. The proposed approach also offers added desing flexibility since it allows for simulation of both positive as well as negative resistors (Fig. 1). Thus, the need for the inverting stage required in the main feedback loop of several well known RC active structures is obviated.

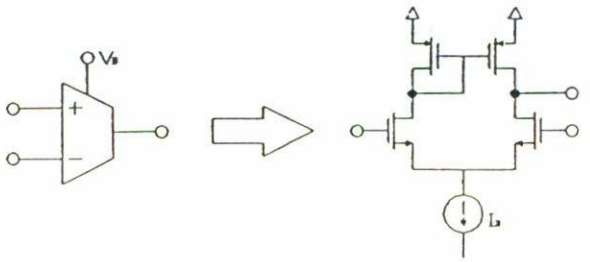

FIGURE 2. Simple OTA implementation

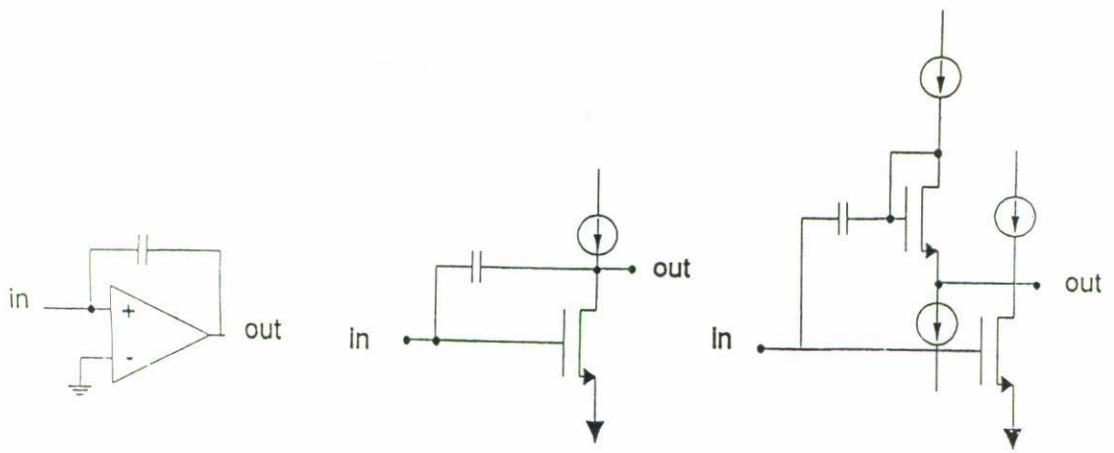

FIGURE 3. (a) Op-amp Miller integrator; (b) simple Miller integrator using a gain stage; (c) active compensated Miller integrator

2.2. Op-amp and integrator simulation

Op-amp integrators are replaced by gain stages with Miller capacitors as shown in Fig. 3. This leads to an integrator with unity gain frequency: $f_0 = \frac{1}{2\pi}\frac{g_m}{C}$ (where g_m is the small signal transconductance gain of a gain stage transistor). Notice that since op-amps are connected only to the high impedance input terminals of OTA simulated resistors, the op-amp does not require current driving capability; and for this reason, it can be reduced to a simple gain stage. It is well known that in this circuit there is a zero in the right half of the s-plane that can introduce significant excess phase at frequencies close to the integrator unity gain frequency leading to Q-enchancement and eventual instability. The conventional compensation technique used to shift this zero to very high frequencies requires a resistor with value $R_z = 1/g_m$ in series with the Miller capacitor. R_z is usually simulated with a MOS transistor in ohmic mode [9]. By using this approach, it is very difficult to match a transistor in ohmic mode to one in saturation; and it makes frequency compensation, in practice, not very effective. An alternative active compensation scheme which uses a diode-connected transistor matched to that in the gain stage is used here instead (Fig. 3c). The small-signal equivalent circuit of this transistor is a resistor with $R_z = 1/g_{mz}$ that can be accurately matched to the value g_m to satisfy the compensating condition. This ensures shifting of the zero to very high frequencies. From simulations of

an integrator with unity gain frequency, $f_0 = 5$ MHz, it has been determined that excess phase at f_0 of less than 0.1° is feasible. An advantage of the proposed approach is that due to the simplicity of the building blocks, the circuit can operate on low supply voltages (single 3.3 V supply).

3. UNIVERSAL OTA-GS FILTER

To illustrate the proposed aproach, a universal filter derived from an RC active prototype is discussed next. Figure 4a shows the block diagram of a second order system characterized by the biquadratic transfer function

$$H(s) = \frac{\text{GHP}\, s^2 + \text{GBP}\, \frac{\omega_0}{Q} s + \text{GLP}\omega_0^2}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2}.$$

Figure 4b shows an RC active implementation of the block diagram of Fig. 4a using the conventional inverting summing and inverting Miller integrator stages. This structure allows independent adjustment for all filter parameters: Q, GLP, GHP, GBP and f_0. It can be translated into an OTA-GS structure with the replacements indicated in Figs. 1 through 3. A disadvantage of this structure is the excess phase introduced by the summing node in the main negative feedback loop which can lead to instability at high frequencies. Figure 4c shows a modification which has the same transfer function and that also allows independent adjustment of all filter parameters; but, with the summing node brought out of the main feedback loop. This is done by including two additional negative resistors with value r_{GHP} (some resistors in the original version require also to be transformed into negative ones). In this modified version, the excess phase of the summing node does not affect significantly high frequency operation. This modification is possible only because of the availability of negative resistors in the presently proposed approach.

4. SIMULATION AND EXPERIMENTAL RESULTS

4.1. Simulation results

Simulations of the OTA-GS filter of Fig. 4c were performed using the building blocks of Figs. 2 and 3c. For the simulations, ±2.5 V supplies, and 2 μm CMOS P-well MOSIS technology parameters were used, capacitors with nominal values of $C = 3$ pF, N-channel transistors with dimensions 6/3 (μm), P-channel transistors with dimensions 10/3, and bias currents of 30 μA were used. Figure 5a shows simulations of the bandpass and notch responses obtained from the same circuit. The filter's behavior is modified by simply adjusting the bias currents of the OTA's simulating resistors: r/GBP, r/GBP and r/GLP so that only the appropriate transductors remain active. Figures 5b and 5c show independent Q and f_0 adjustment (with the bias currents of the OTAs simulating r_Q and R). The universal filter was laid out (Fig. 6) for 2 μm P-well CMOS technology and it is currently being fabricated by MOSIS. The area of the filter is 360 × 400 μm^2, the total power disipation is 2.5 mW.

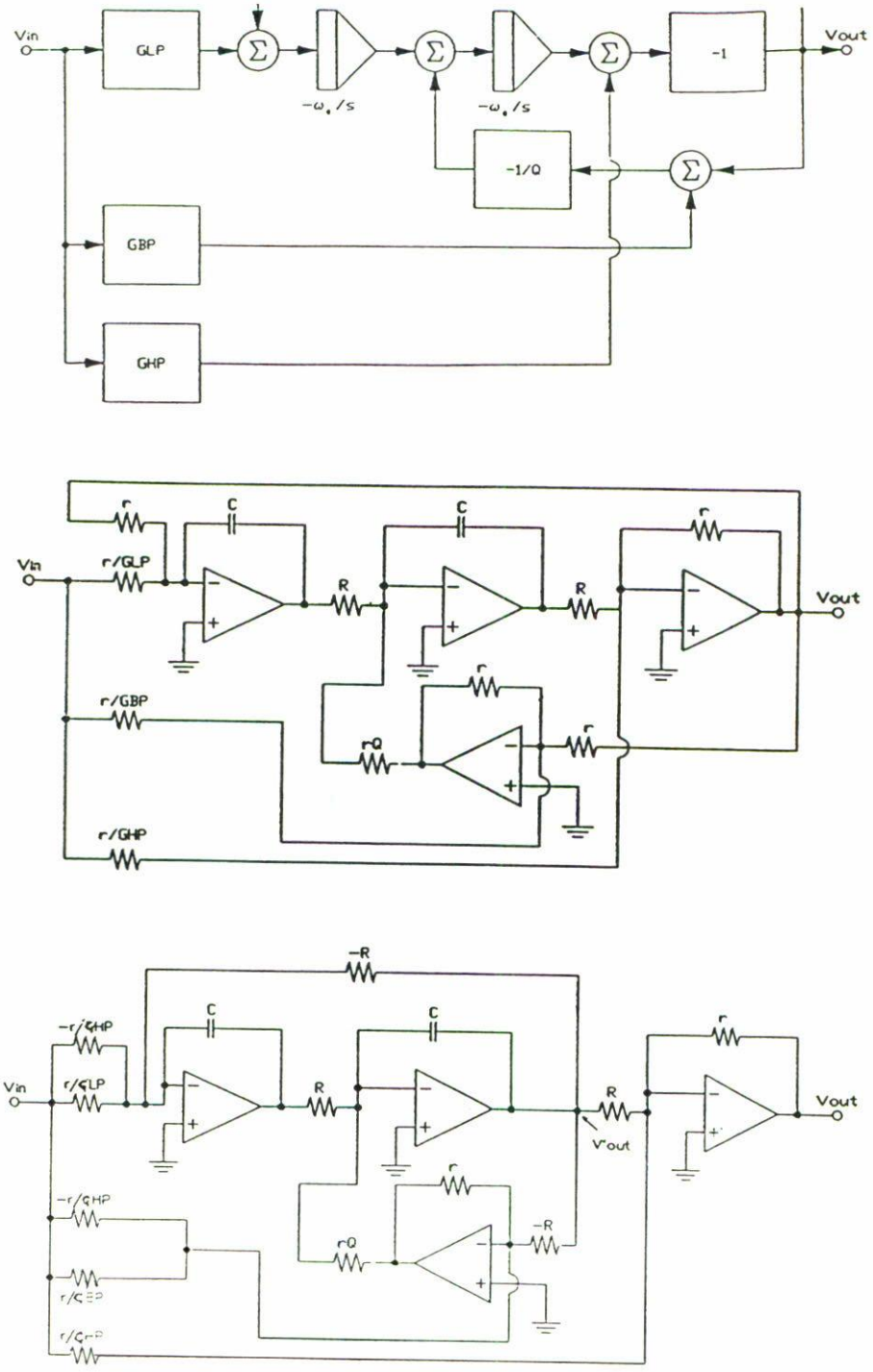

FIGURE 4. (a) Block diagram of biquadratic system; (b) RC active universal filter; (c) high frequency modification of RC active universal filter.

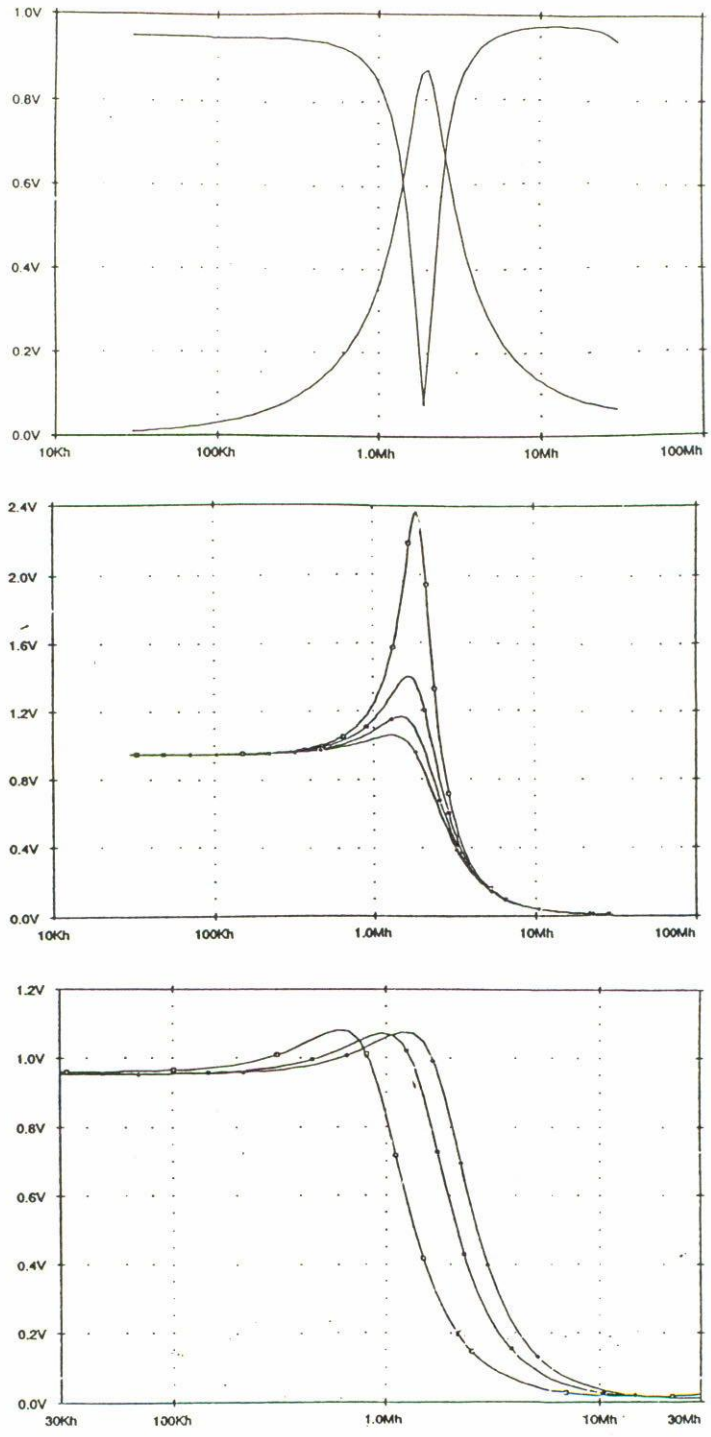

FIGURE 5. SPICE Simulated frequency response of CMOS implementation of circuit of Fig. 6c: (a) Bandpass and notch responses; (b) low-pass response with variable Q; (c) low-pass response with variable f_0.

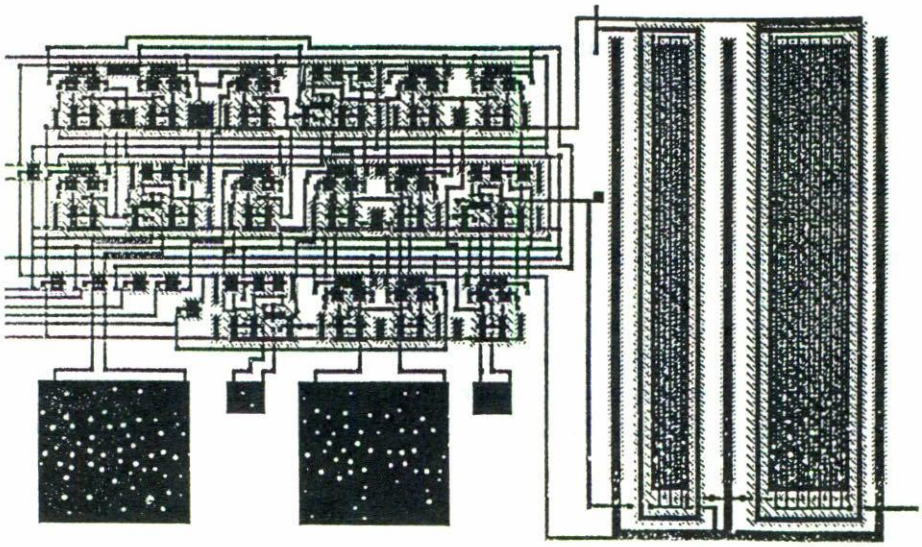

FIGURE 6. Layout of fabricated CMOS universal filter.

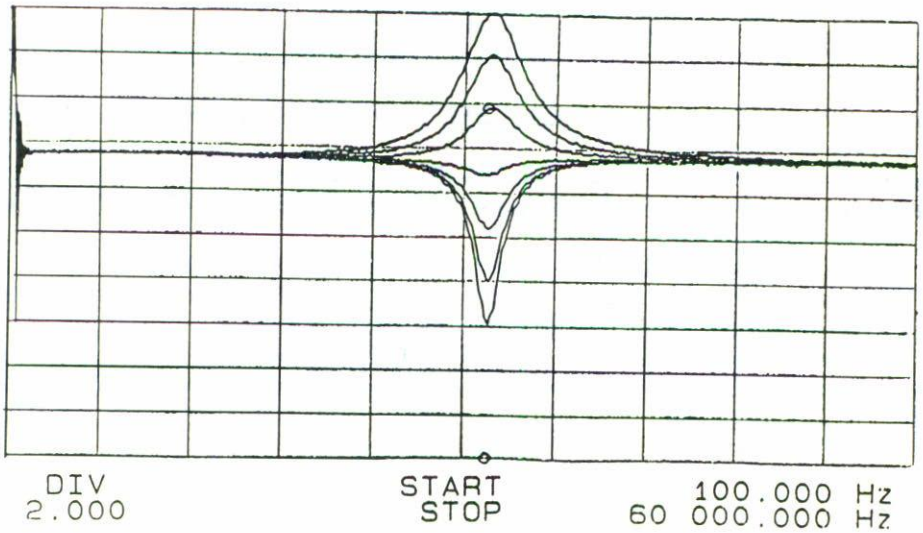

FIGURE 7. Experimental bump equalizer response.

4.2. Experimental results

To verify the proposed concept, a breadboard prototype of the universal filter of Fig. 5b was built using bipolar OTAs (CA3280) for resistor simulation and 741 op-amps for Miller integrator implementation. All OTAs were biased to simulate 20 kΩ resistors with exception of the OTA simulating rQ that was biased to simulate a 100 kΩ resistor so that a nominal $Q = 5$ would be obtained. 1000 pF ceramic capacitors were used. A pole frequency, f_0, of approximately 30 kHz was obtained. Figure 7 shows the experimental bump equalizer's response obtained by setting equal low-pass and high-pass gain coefficients: GLP, GHP = 1; and by varying the band-pass gain coefficient, GBP. Independent Q and

f_0 adjustments were experimentally verified to be in good agreement with simulations (scaled down by frequency factor ~ 100).

5. CONCLUSION

An approach which allows to derive CMOS integratable filters from conventional RC active structures was presented and experimentally verified. Techniques for high frequency compensation were discussed and illustrated with a universal filter. Future work in this area contemplates the simulation of resistors with four quadrant transconductance multiplier cells to provide filters with wide range programmable characteristics, the design of fully differential structures and the utilization of floating gate devices to reduce supply requirements to ± 0.75 V.

REFERENCES

1. R. Schaumann, M.S. Ghausi, and K.R. Laker, *Design of analog filters, passive, active RC and switched capacitor*, Prentice Hall, Englewood Cliffs (1990).
2. A. Sedra and P.O. Bracket, *Filter theory and design: active and passive*, Matrix Publishers (1978).
3. M. Ismail, S.V. Smith, and R.G. Beale, *IEEE J. of Solid State Circuits*, SC-23 (Feb. 1988) 183.
4. M. Banu and Y.P. Tsividis, *IEEE J. of Solid State Ciruits*, SC-20 (Dec. 1985) 1114.
5. J.M. Khoury and Y.P. Tsividis, *IEEE Trans. on Circts. and Syst.*, CAS-34, No. 88 (Aug. 1987) 863.
6. K. Vavelidis and Y.P. Tsividis, *Proc. of IEEE-ISCAS*, Chicago (May 1993).
7. S.D. Willingham and K.W. Martin, "BiCMOS Component for video rate continuoustime filters" in *Proc. of IEEE-ISCAS*, London (May 30-June 2, 1994).
8. J. Ramírez Angulo, *Electronics Letters* **28**, No. 19 (Sept. 1992) 1783.
9. R. Gregorian and G.C. Temes, *Analog MOS integrated circuits for signal processing*, J. Wiley and Sons, New York (1986).