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Influence of oxide surface charge on the sine-voltage sweep C-V measurements

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ABSTRACT. The influence of a negative mobile charge on the outer oxide surface of MOS (metal oxide semiconductor) structures on the C-V measurements performed by the sine-voltage sweep C-V method was investigated. It was found that this charge induces changes on the depletion capacitance, which results in a specific form of Zerbst plot. This fact can be used as an indication for the existence of this kind of instability and that the final results of the measurements can be affected.

RESUMEN. La existencia de carga negativa móvil en la superficie exterior del óxido de silicio, influye de manera negativa sobre las características C-V obtenidas usando el método de barrido de voltaje senosoidal en estructuras MOS. Encontramos que esta carga provoca un cambio en la capacitancia de deserción, la cual da como resultado un cambio específico de la curva Zerbst. Este hecho puede ser usado como un indicativo de la existencia de carga negativa sobre el óxido. Los valores de los parámetros obtenidos de la curva Zerbst, S (velocidad de generación superficial) y τ_g (tiempo de vida de generación), bajo estas circunstancias, no serán correctos.

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1. INTRODUCTION

It is well known that a negative charge on the outer oxide surface of MOS (metal oxide semiconductor) devices can be formed in the presence of moisture [1, 2]. In the presence of an electric field this charge can be responsible for a current flow along the oxide surface. The exact mechanism for moisture induced current flow is unknown. However, it was supposed that small amounts of contamination (salt compounds principally) may pick up from environment during the final processes and/or measurements of the MOS devices. In addition, if humidity in the ambient exists a film of water can be adsorbed on the top oxide surface. Because water has a high dielectric constant, surface contaminants become ionized into a separate anion and cation [3]. If bias is applied to the device an ionic current can flow along of the oxide surface.

Recently a sine-voltage C-V method for determination of generation lifetime and surface generation velocity was proposed [4]. In the present work the influence of a mobile negative charge at the outer oxide surface of MOS structures on the sine-voltage sweep C-V characteristics is investigated.

2. Sample preparation and measurements

MOS capacitors were fabricated on n-type 2–5 Ω cm, (100) oriented, CZ grown Si wafer. The wafer was cleaned by the standard RCA process. The oxidation was performed at 1000°C in dry O_2 + 2% TCA ($C_2H_3Cl_3$) to obtain 1000 Å thick oxide. The wafer was annealed at the same temperature in dry N_2 for 30 min. The backside oxide was removed. Aluminum dots for MOS capacitors were deposited through a metal mask on the top oxide. On the backside of the wafer, aluminum was also evaporated and the wafer was sintered in a N_2/H_2 ambient at 425°C for 30 min.

The sine-voltage C-V method [4] was used in this experiment. The h.f. (high frequency) C-V curves were measured with a Boonton 72B capacitance meter at 1 MHz. A Wavetek model 271 function generator was used as a sine-voltage source. The measurements were performed at room temperature in the following way. On the gate electrode a sine voltage with the form $V = V_a \sin(\omega t)$ was applied, where V_a is the voltage amplitude, ω is the angular frequency and t is the time. In the first experiment on the gate electrode of the MOS structure only the negative half cycle of the sine voltage was applied, changing the voltage amplitude V_a and keeping the frequency constant so that $V(t = 0) = 0$ and $V_{G_{max}} = -V_a$. In the second experiment the complete sine voltage signal was applied on the gate electrode so that $V_{G_{max}} = \pm V_a$.

3. Experimental results and discussion

First of all, let us analyze the above mentioned experiments. In the first case, the negative voltage pushes away the negative charge from the gate electrode. This negative charge on the outer oxide surface increases both the lateral depleted surface area in the semiconductor (n-type) and the net lateral surface generation rate. In order to compensate for the increased lateral surface generation rate, the depletion region generation decreases and thus the measured capacitance increases [5].

In the second case, the negative half cycle influences in the same way but the positive one produces a motion of the negative charge towards the gate electrode. The sum of the influence of these two half cycles results in less negative charge on the outer oxide surface, smaller lateral depleted surface area, lower net surface generation rate, increasing of the depletion region width and finally the measured capacitance is lower compared with the previous case.

In Fig. 1 sine voltage sweep C-V curves for these two cases are presented. As shown in Fig. 1, the application of only negative half cycle results in higher C_{sat}, where C_{sat} is the minimum capacitance (or the capacitance in the point of the C-V curve where $dC/dV = 0$).

According to the sine voltage sweep C-V method [4] we can write

$$R = \frac{dV}{dt} = V_a \omega \cos(\omega t) = \frac{q n_i K_s}{C_{ox} C_{inv} \tau_g} \left(\frac{C_{inv}}{C_{sat}} - 1 \right) + \frac{q n_i S}{C_{ox}},$$

where C_{ox} is the oxide capacitance, C_{inv} is the quasi-equilibrium inversion capacitance, S is the surface generation velocity, n_i is the intrinsic carrier concentration, K_s is the

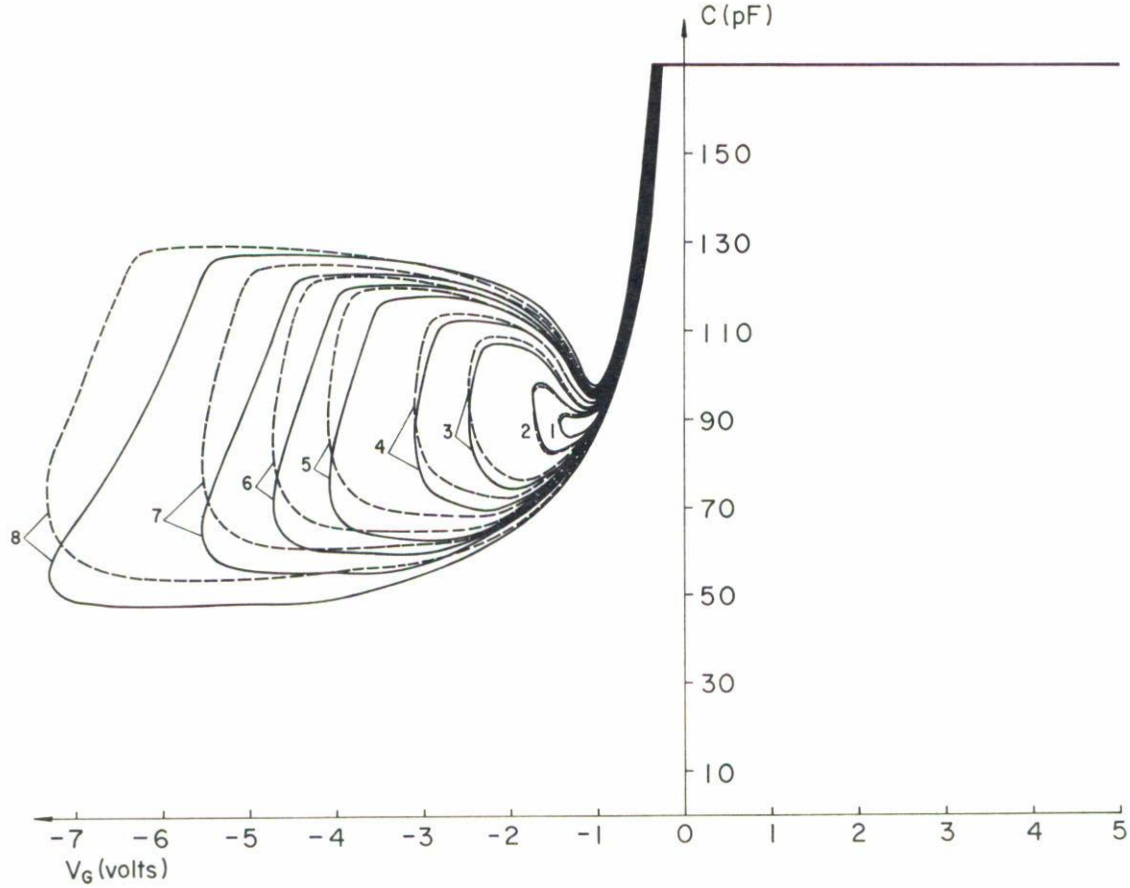

FIGURE 1. Experimental h.f. sine-voltage C-V curves. - - -: Negative half cycle applied; —: Negative and positive half cycles applied.

permittivity of the silicon, q is the charge of electron, τ_g is the generation lifetime, ω is the angular frequency and t is the time.

Using the data from Fig. 1 and the above equation, the so called Zerbst plots (R *vs.* $(C_{inv}/C_{sat}) - 1$) for these two cases were obtained and it is shown in Fig. 2. The slope of the linear part of this plot is proportional to $1/\tau_g$ and the intercept of its extrapolated linear part is proportional to S. From Fig. 2 it can be seen that only when the negative half cycle is applied on the gate electrode a distortion of the Zerbst plot is observed. The distortion of the Zerbst plot can provoke the disappearance of its linear part or change of its slope. This distortion has a specific form and this fact can be used as an indication for the existence of a current flow along the oxide surface.

As mentioned before, residual contaminants can be ionized and separated into anions and cations through an adsorbed water layer. It might be the origin of the negative charge on the top oxide surface. The room ambient may be one of the sources of humidity, so that, in order to avoid this effect, we should previously dry flowing N_2 on the samples and keep the wafer in same ambient, while the measurements are performed.

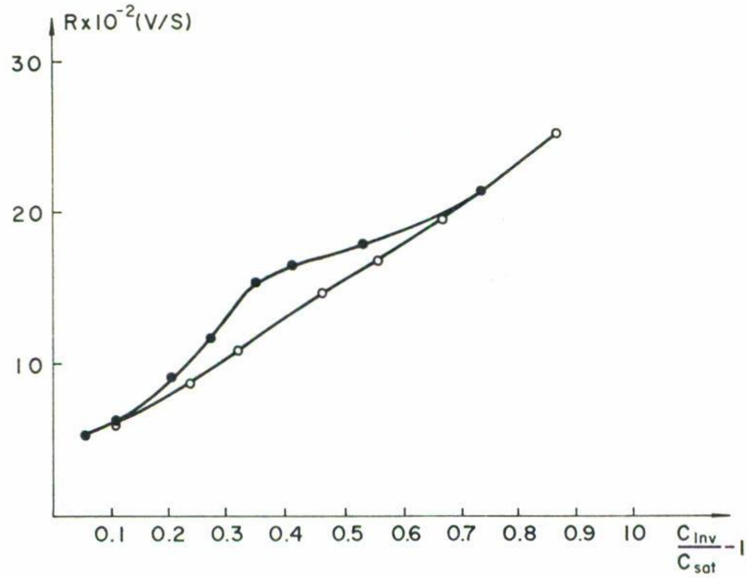

FIGURE 2. Zerbst plot, R *vs.* $((C_{\rm inv}/C_{\rm sat})-1)$. •: Negative half cycle applied; o: Positive and negative half cycles applied.

4. CONCLUSIONS

In conclusion it can be said that the existence of a negative charge on the outer oxide surface affects the shape of the Zerbst plot obtained from the sine-voltage C-V curves. For small distortions of the Zerbst plot the values of generation lifetime and surface generation velocity will be incorrect, while for large distortions it will be impossible to obtain them. The distortion of the Zerbst plot can be used as an indication for the presence of negative charge on the outer oxide surface. To avoid this effect, the sample must be held in dry N_2 ambient during the measurements.

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