Silicon supports for condenser microphone applications

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Silicon supports have been fabricated in standard IC fabrication process using a very simple method. The application of silicon supports in the design of a fully integrated condenser microphone is experimentally presented. The method is absolutely planar and does not require any extraordinary steps during the fabrication process. The significant points of the proposed microphone are a very large number of ventilation holes in the backplate (1.3×1.3 mm^2) allowing a small air-gap ($1.5\ \mu$m) and an integrated backchamber ($25\ \mu$m depth).

Keywords: Silicon etching; surface micromachining; KOH

Usando un método simple, se han fabricado soportes de silicio usando un proceso de fabricación estándar de CI's. Experimentalmente se demuestra que los soportes de silicio tienen aplicación en el desarrollo de micrófonos de condensador completamente integrados. El método propuesto de diseño es absolutamente planar y no requiere de una secuencia compleja durante su implementación. Los aspectos más importantes del micrófono que se propone son la integración de una densidad de perforaciones en la placa fija (1.3×1.3mm^2), así como una separación de placas de $1.5\ \mu$m y la integración de una micro-cámara de $25\ \mu$m de profundidad.

Descriptores: Grabado de silicio; micromaquinado de superficie; KOH

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1. Introduction

Although hillocks have been reported as a common irritant creation of micromechanical devices, it is an interesting exercise to determine some hillock fabrication sequence to have control of its dimensions and using the resulting structures in practical transducers. In this paper we show how a condenser microphone can be developed using silicon pyramids to build both a backchamber and a perforated silicon nitride backplate. The paper is organized as follows. A simple method to fabricate silicon pyramid (or silicon supports) is shown in Sect. 2. Fabrication of silicon pyramids using standard IC fabrication process is presented in Sect. 3. Silicon supports' application in a fully integrated condenser microphone and its simulation using a mechano-acoustic lumped parameter model are discussed in Sect. 4. At the end of the paper the conclusions are given.

2. Procedures of proposed method

An ideal silicon pyramidal shape is bounded by (111) surfaces, which means that its fabrication must include a pattern rotated 45° respect the primary flat in a (100) n-type silicon wafer as shown in Fig. 1. That is suitable because the etch rate in silicon is about 200 times larger on the (100) and 400 times larger on the (110) than on the (111) surfaces in KOH (potassium hydroxide and DI water) [1]. In practice, the fabrication of silicon pyramidal shape results in a hillock or a near-pyramidal shape, which is bounded by sharply defined convex edges and near-(111) surfaces [2]. Figure 2 shows an idea of silicon pyramid formation process. First a cavity toward pyramidal shape is formed by undercut-etching the silicon substrate (see Fig. 2a). After sufficient silicon etching has occurred the neighbor etched holes intersect each other resulting in a flat-top silicon pyramid (see Fig. 2b).

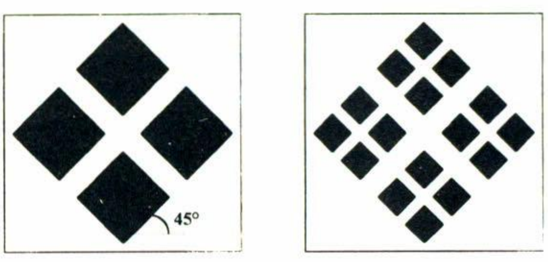
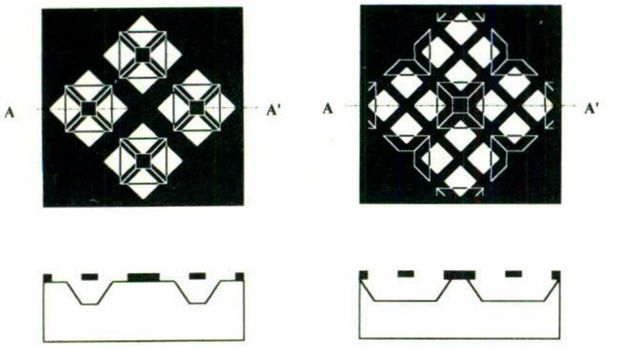


FIGURE 1. a) Basic cell to develop a silicon pyramidal shape and b) basic cell to built Mask-1.

3. Fabrication process

The fabrication sequence begins with the use of n-type, 1–5 $\Omega\cdot$cm, $\langle 100\rangle$ 3-in silicon wafers. All technological steps, typical for the CMOS LSI, were performed with the use of IC technological line and photolithography masks with a minimum line definition of $5\ \mu$m. The wafers were prepared for



(a) (b)

FIGURE 2. An idea of silicon pyramidal formation process (black color: nitride, white color: silicon).

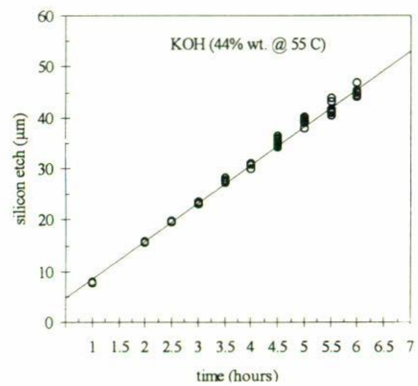
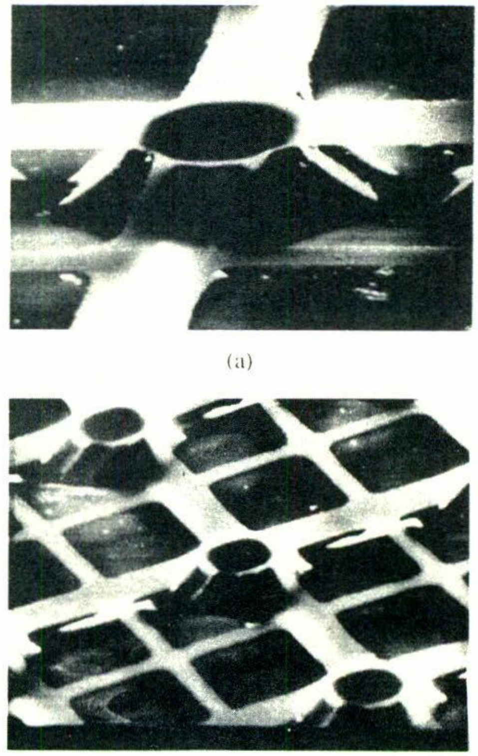


FIGURE 3. The silicon etch rate is of the order of 0.129 μm/min for the (100) plane. There are over 100 data points on the graph, although they are not all visible due to overlapping. (Note: line is the result of a linear regression).

silicon nitride deposition (160 nm LPCVD-Si_3N_4 at 700°C) by a standard RCA cleaning procedure. The wafers were spin-coated with a layer of positive photoresist and patterned with mask 1 (see Fig. 1b). The nitride layer was then etched using phosphoric acid at 150°C. In our experiment the silicon is etched in a 44% (by weight) KOH solution at 55°C (see Fig. 3). The temperature was keep constant by a Blue M constant temperature bath, within ±1°C by mean of a proportional electronic temperature control unit. This temperature and concentration were chosen to minimize loss of water due to evaporation. Figure 4a shows a scanning electron micrograph (SEM) of the resulting structure, illustrating the flat-top hillock (FTH) of 25.0 μm height, which was measured using a Leitz ORTHOPLAN optical microscope with a micrometer screw for fine focusing. The microscope was equipped with a mechanical stage with micrometer screws graduated for adjustment in X and Y directions. Figure 4b shows an open view of the resulting structure. The length of the visible Si_3N_4 beams between FTH's (or silicon supports) is 90 μm and its width is 20 μm. The narrow floating Si_3N_4-elements have a width of 10 μm and the windows are 40× 40 μm^2 each.



(a)

(b)

FIGURA 4. a) close-up of a silicon support and b) SEM micrograph of silicon supports after 3.5 h in 44% (by weight) KOH at 55°C.

4. Condenser microphone design

Typical data are listed in Table I for microphones reported up to now [3–26]. The piezoelectric microphone contains a transducer element that generates a voltage when mechanically deformed. The voltage is proportional to the displacement in the frequency range below the resonance of the element [4, 10, 27]. The condenser microphone has enjoyed the highest degree of success due to its superior signal-to-noise ratio, high sensitivity, low temperature coefficient and long-term stability. Condenser microphones are divided into two classes: externally polarized or prepolarized (electret). Because a condenser microphone depends for its operation on variations in its internal capacitance, the function of the polarizing voltage, or its equivalent, is to translate the diaphragm motion into a linearly related audio output voltage, which is amplified by a preamplifier [28]. As Table I shows, the electret approach has an open-circuit sensitivity up to 25 mV/Pa. Disadvantages of those designs are poor retention of the electric charges and hybrid technology with Mylar diaphragms. Furthermore, the Mylar foil is attached manually on the silicon wafer with the backplate and fixed by a polymer spray [5]. In some cases, the bias of the microphone is supplied with an external voltage source and other approaches have been presented, characterized either by multi-wafer assemblies using bulk micromachining techniques [6–8, 11, 12, 14]. This approach can be very laborious

TABLE I. Micromechanical silicon microphones. dBA is the noise level that is measured using an A-weighing filter, in dB relative to 2×10^{-5} Pa, which is the lowest sound level detectable by the human ear. The A-weighing filter corrects for the frequency characteristic of the human ear, thus providing a measured of the audibility of noise.

Author, year [Ref.]	Transducer principle	Diaphragm material size	Resonance frecuency (kHz)	Sensitivity (mV/Pa)	Equivalent noise level (dBA)	Capacitance or impedance
Hohm, 1984 [3]	electret 2 μm SiO_2	13 μm Maylar 8 mm diam	8.5	8.8		9 pF
Muller, 1987 [4]	piezoelectic 0.3 μm ZnO	2 μm nitride 3×3 mm^2	7.8	0.5		
Sprenkels, 1989 [5]	electret 1.1 μm SiO_2	2.5 μm Maylar 0.6×0.6 mm^2		25		
Bergqvist, 1990 [6]	condenser 16 V bias	5 μm silicon 3×4 mm^2		13		3.5 pF
Kühnel, 1991 [7]	FET 30 V bias	100 μm nitride 1×1 mm^2		1	$1/\sqrt{f}$ dependence	
Bergqvist, 1991 [8]	condenser 5 V bias	5.1 μm silicon 2×2 mm^2	27	1-2	37-44	5 pF
Scheeper, 1991 [9]	condenser -2 V bias	1.0 μm nitride 2×2 mm^2		1.4		
Kim, 1991 [10]	piezoelectic 0.5 μm ZnO	2 μm nitride 3×3 mm^2				
Kühnel, 1992 [11]	condenser 28 V bias	100 nm nitride 0.8×0.8 mm^2		1.8	< 25	1.3 pF
Bourouina, 1992 [12]	condenser 20 V bias	1 μm doped Si 1×1 mm^2	120	3.5	38	
Schellin, 1992 [13]	piezoresistive 6 V bias	1 μm silicon 1×1 mm^2	10	0.025		
Kühnel, 1992 [14]	condenser 28 V bias	150 nm nitride 1×1 mm^2	16	3		
Scheeper, 1992 [15]	condenser 16 V bias	1 μm nitride 1.5×1.5 mm^2		1	22	7 pF
Ried, 1993 [16]	piezoresistive 0.5 μm ZnO	2 μm nitride 2.5×2.5 mm^2	18	0.92		
Bergqvist, 1994 [17]	condenser 28 V bias	8 μm silicon 1.8×1.8 mm^2	14	1.4		5.4 pF
Bergqvist, 1994 [18]	condenser 0-9 V bias	5 μm silicon 2×2 mm^2		0-7.5	33-30	6.4 pF
Kälvesten, 1995 [19]	piezoresistive 10 V bias	0.4 μm poly-Si 0.1×0.1 mm^2	1.31	0.9	96	
Schellin, 1995 [20]	piezoresistive 8 V bias	1.3 μm silicon 1×1 mm^2	> 20	0.08	61	
Horwarth, 1995 [21]	condenser 2 V bias	0.2 μm silicon 0.2×0.2 mm^2		0.3		
Kovács, 1995 [22]	condenser 5 V bias	1.5 μm polySi 0.5×0.5 mm^2	26	0.065	58	
Kronast, 1995 [23]	FET 9 V bias	4.5 μm silicon 1×1 mm^2	53	0.04		
Ning, 1996 [24]	condenser 6 V bias	1 μm nitride 2×2 mm^2		7		9.5 pF
Bay, 1996 [25]	condenser	0.2 μm nitride 2×2 mm^2				
Hsieh, 1997 [26]	electret 1.2 μm teflon	0.91 μm nitride 3.5×3.5 mm^2	38	0.2	60	5.2 pF

when carrying out alignment procedures and wafer bonding, which often reduces the overall device yield. Finally, the FET-microphone, when the diaphragm act a mobile gate in a field effect MOS transistor present other difficulties, such as instability due the unprotected region, and $1/f$ noise due the implanted channel [11, 23]. Actually, the so-called second generation of condenser microphone uses silicon micromachining techniques and no bonding techniques are required. In that sense Scheeper *et al.* [15] constructed a condenser microphone using a single wafer process. That process is based on the sacrificial layer technique. The sacrificial aluminum layer is etched through access holes that are anisotropically etched from the reverse side of the wafer. These access holes act as acoustic holes during normal operation of the microphone. As the backplate is perforated, the damping (due to volume air into the air-gap) can be reduced considerably as the air can escape through the perforations. On the other hand, Bergqvist and Gober [17] fabricated a condenser microphone with a backplate constructed by electrodeposition of copper on a sacrificial photoresist layer. The microphone diaphragm is monocrystalline silicon and is fabricated with anisotropic etching of the substrate wafer. In practice, using aluminum sacrificial layer requires an elaborated freeze-drying follow-up process to prevent the diaphragm from sticking to the backplate. On the other hand, electroplating technology does not allow any higher temperature process after the photoresist has been deposited.

In this paper we show how a condenser microphone can be developed using silicon pyramids to build both a backchamber and a perforated silicon nitride backplate. The proposed method does not require any extraordinary steps during the fabrication process, that is, deep substrate etching from the back side of the wafer to form a diaphragm or a backplate, silicon-to-silicon or silicon-to glass bonding to form the sensor chamber, diaphragm positioning, and so on. The proposed structure shown in Fig. 2 can be used as the base to fabricate a nitride-polisilicon-nitride (NPN) perforated backplate of a condenser microphone. Figure 5 shows an idea of the proposed backplate. In the IC fabrication process at INAOE the polisilicon (poly-Si) gate layer is heavily doped with phosphorus to minimize its sheet resistance, and is well know that phosphorous doping negatively affects stress in poly-Si layers during high-temperature annealing [29]. To reduce that stress the nitride films counteract the compressive internal stress in the poly-Si layer and make possible longer microbridges. On the other hand, as the capacitance of the microphone must be greatest that parasitics the necessary length of the poly-Si bridges is about 600 μm each. As we can see the NPN integrity can be maintained by the FTH's. Moreover, the gap between silicon and NPN constitutes the height of a backchamber, which reduces the air-gap damping. Finally, the air-streaming resistance of the air-gap is a function of the open-windows nitride density. To increase that density we have used the mask 1 to define four open-windows into the area defined by four FTH neighbors. To complete the transducer design we have used the sacrificial layer technique to obtain the air-gap height and the movable plate or diaphragm. Phosphosilicate glass (PSG) is used to offset the nitride diaphragm from the backplate. A second layer of PSG is used as mechanical support. Figure 6 shows a schematic representation of the full fabrication process. As we can see in Fig. 6b etch-holes are formed such as to penetrate the silicon nitride layer to reach the sacrificial PSG. After etching sacrificial PSG the silicon substrate is anisotropically etched through the etch-holes, thereby forming the perforated backplate and the backchamber (see Fig. 6c). Before the metalization step, oxide is deposited to seal the etch-holes by CVD process. Figure 7 shows a photograph of the fully integrated condenser microphone. In practice, the diaphragm deflection must be independent of the atmospheric pressure, and then the microphone has to be equipped with a vent channel to equalize the static air pressure difference between the cavity and the ambient. In the proposed microphone an etching hole is designed as an equalization hole. However, as the atmospheric pressure, P_o, is present at both sides of the diaphrag the mechanical sensitivity is reduced to [30]

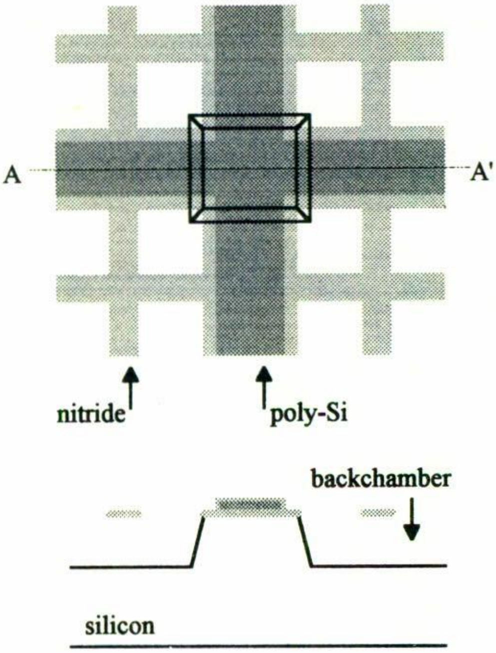


FIGURE 5. Idea of the proposed perforated backplate (not to scale).

$$S_m = \frac{\partial W_P}{\partial P} = \frac{1}{30\frac{D}{A}\sigma_R + \frac{P_0}{d_0}}, \qquad (1)$$

where W_P is the average diaphragm displacement, P the applied pressure, d_0 the thickness of the backchamber, σ_R the residual stress of the diaphragm material, D the total diaphragm thickness and A its area. As residual stress is a constructional parameter that can be varied, its value is essential in increasing the sensitivity of the diaphragm. In practice, silicon nitride (as well as most of the thin films being used in IC processing) exhibit stress that can be tensile or compressive.

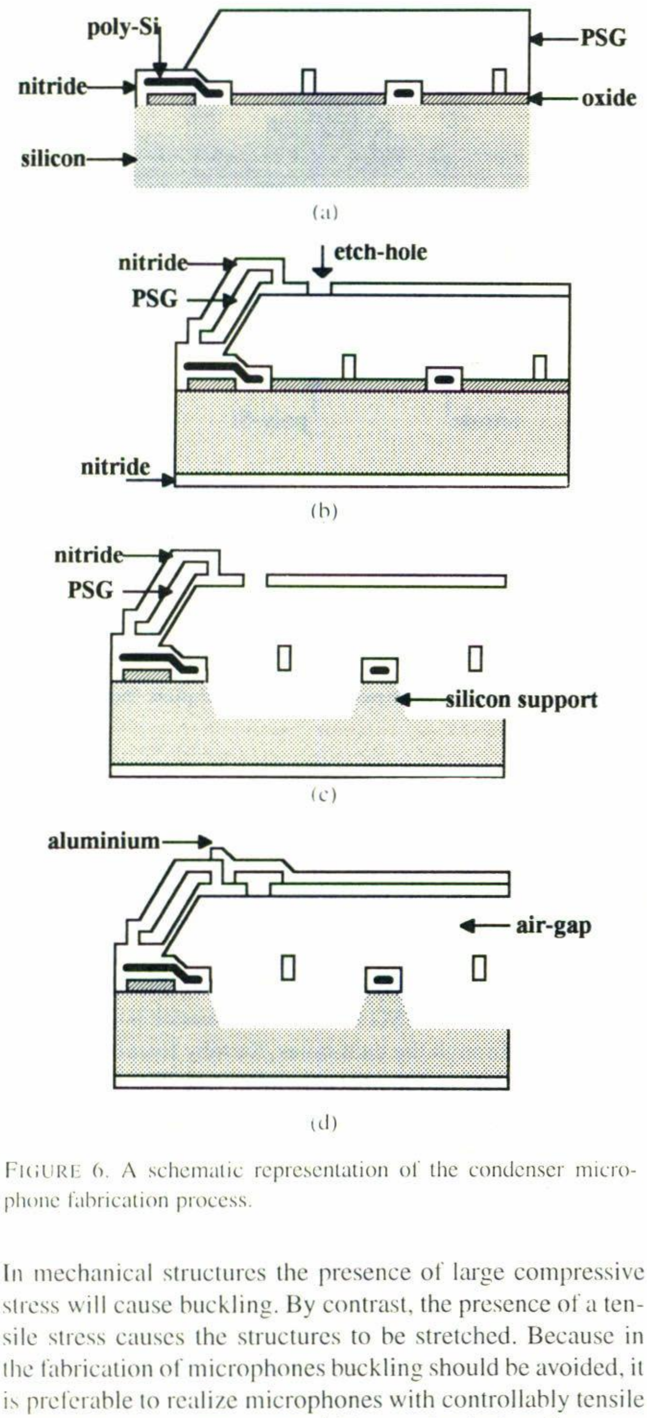


FIGURE 6. A schematic representation of the condenser microphone fabrication process.

In mechanical structures the presence of large compressive stress will cause buckling. By contrast, the presence of a tensile stress causes the structures to be stretched. Because in the fabrication of microphones buckling should be avoided, it is preferable to realize microphones with controllably tensile stress. But, it is advantageous if the mechanical performance of the diaphragm is not too critically determined by deposition process parameters. A suitable method to achieve this is by using boron implantation. In our experiment the nitride layer was processed with a dose from 3×10^{14} cm^{-2} to 1.2×10^{15} cm^{-2}, and the ion energy was chosen in such a way that a peak of the defect concentration was placed in the middle of the layer thickness. Thus, for 180 nm thick silicon

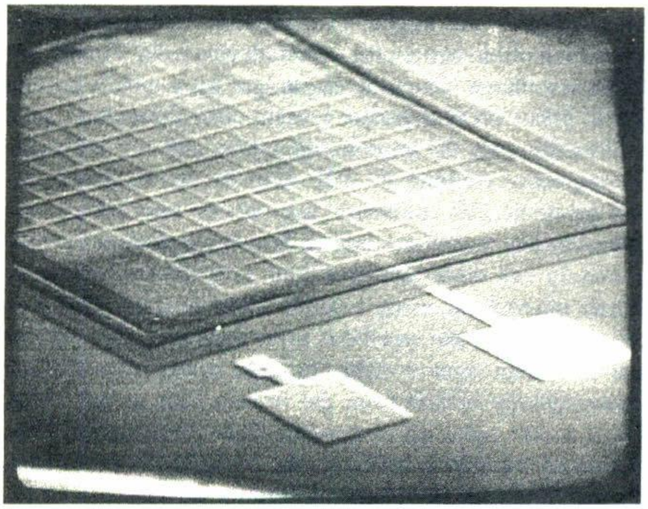


FIGURE 7. Photograph of the fully integrated condenser microphone.

nitride an implantation energy of 65 keV was deduced. It is important to say that the method for measuring both compressive and tensile stress was based on the so-called *buckling technique*.

5. Conclusions

A simple method to fabricate silicon hillocks has been presented. The proposed method is compatible with standard IC fabrication process and does not require any special steps during the fabrication process, that is, deep substrate etching from the back side of the wafer to form a diaphragm or a backplate, silicon-to-silicon or silicon-to glass bonding to form the sensor chamber, diaphragm positioning, and so on. Furthermore, as the proposed method is absolutely planar we have used the silicon hillocks as supports in a fully integrated condenser microphone. In this application the silicon hillocks constitute the base to develop a backchamber and a perforated backplate. Thus, the damping (due to volume air into the air-gap) can be reduced considerably as the air can escape through the perforations. The useful of the silicon hillocks have been demonstrated in a practical transducer. The analysis of the electroacoustic experimental data will be presented in a future paper.

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