Influence of segregation annealing time on the gettering process

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The influence of segregation annealing time on the gettering efficiency of phosphorous ion implantation gettering in MOS structures was investigated. The gettering was performed by a backside P ion implantation with a dose of 10^{16} atoms/cm^2 and 120 KeV energy. To investigate the gettering efficiency, surface generation velocity and 3-dimensional generation lifetime profile as a function of the annealing time were investigated. It was found that there is an optimum annealing time for maximum gettering efficiency. Surface generation velocity and generation lifetime increase for annealing less or equal to the optimum annealing time, which was 90 min for our case. For longer annealing times both parameters deteriorate. The analysis of the results shows that the increase of generation lifetime and the decrease of surface generation velocity are due to a gettering of metallic impurities and shrinkage of oxidation stacking faults (OSFs). The deterioration of these parameters for annealing times longer than the optimum annealing time is explained by the combined influence of OSFs shrinkage, release of the captured metallic impurities from gettering sites in the damaged implanted region and by metallic impurities contamination from the furnace. The concept of the optimum annealing time is incorporated in the segregation model of the gettering process.

Keywords: Silicon; gettering; ion implantation; lifetime

Se investigó la influencia del tiempo de recocido sobre la eficiencia de *gettering* en estructuras MOS. Se estudió la eficiencia de *gettering* por implantación de fósforo por la parte de atrás de la oblea con dosis de 10^{16} atm/cm^2 y 120 KeV de energa de implantación. Para determinar la eficiencia de *gettering*, se usó la variación con el tiempo de recocido del tiempo de vida de generación y la velocidad de generación superficial. Se encontró que existe un tiempo óptimo de recocido, donde se obtiene el máximo tiempo de vida, y en nuestro caso fue de 90 min. El tiempo de vida aumenta y la velocidad superficial disminuye con el tiempo de recocido hasta el tiempo óptimo. Para tiempos mayores al óptimo, ambos parámetros se deterioran. El *gettering* de impurezas metálicas y la reducción de fallas de apilamiento por oxidación (OSF) son los mecanismos responsables del aumento del tiempo de vida y la reducción de la velocidad superficial. La deterioración de los parámetros mencionados, se explica por los efectos combinados de la liberación de impurezas de los sitios de *gettering* en la región implantada, la reducción de los OSF y la difusión de impurezas metálicas del mismo horno de recocido. Por último, el concepto del tiempo optimo de recocido es incorporado en el modelo de segregación del proceso de *gettering*.

Descriptores: Silicio; *gettering*; implantación ionica; tiempo de vida

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1. Introduction

It is well known that metallic impurities and extended defects, especially when decorated with metals, can introduce generation-recombination (G-R) centers. The G-R centers increase the leakage current and reduce recombination and generation lifetime of semiconductor devices.

Gettering is a process that reduces or eliminates metallic impurities in a wafer by localizing them away from the device active regions [1, 2]. Gettering of metallic impurities in silicon is widely used to improve the electrical characteristics and to achieve a high fabrication yield of integrated circuits (IC). Various gettering techniques have been developed: chlorine oxidation [3–5], diffusion [6], silicon nitrite deposition [7], intrinsic gettering [8], mechanical damage [9], ion implantation [10–15], etc. The gettering technique can represent up to 10% of the total IC manufacturing cost.

In spite of the fact that the desired circuit properties and production yield has been achieved to some extend by gettering techniques, the exact mechanism(s) by which gettering come out are still not well understood [12, 16, 17].

The need for improved substrate properties in the coming gigascale integration era, reflected in the requirements of Semiconductor Industry Association Roadmap for the year 2001 [18], results in an increased interest in the gettering [1, 2]. The 0.18 μm generation of devices will require the impurity level in the active device regions to be reduced below 1×10^{10} cm^{-3} and material specification may be as low as 10^8 per cm^{-3} [18].

Among all gettering techniques the ion implantation gettering has received attention due to its ability to produce radiation damage in a very controllable and reproducible way. Different ions have been used to create ion damage [10]. However, to respond to the new requirements it is neces-

sary a comprehensive understanding of defect evolution upon implantation and annealing. That is a severe scientific challenge since it requires the assessment of complex phenomena such as bulk and surface defect recombination, defect clustering and defect-impurity interaction [19]. Moreover, such an assessment must be done for different combinations of substrates and implanted ions.

Nowadays, the efforts are directed towards better understanding of the gettering process [19, 20], optimization of the existing gettering techniques [21–23] and development of new ones [24–30].

In most of the gettering techniques a high temperature annealing is used to insure impurity release, diffusion, and capture at the gettering sites [31–34]. That is why this parameter is of great importance for the gettering efficiency. Usually the annealing is performed in neutral ambient. This means that the annealing temperature and the annealing time will be the parameters affecting the gettering efficiency. Kang and Schroder [35] investigated the role of the annealing temperature and have shown that a optimum one exists. Gao *et al.* [28] have investigated one and two step annealing. Koveshnikov *et al.* [22] have investigated the role of annealing temperature on the gettering of iron in MeV Si implanted into Si, and they have been surprised that release and capture of impurities at different damaged regions is possible with the annealing time. However, it has been already shown that such release of impurities is possible for long annealing time [36]. It is obviously that the annealing time can not be a parameter arbitrarily chosen.

In this work, analyzing the evolution of quasi 3-dimensional profile of generation lifetime and surface generation velocity with the annealing time, we have investigated its role on the gettering efficiency of phosphorous ion implantation gettering in MOS structures. We show in the present case that an optimum annealing time exists. The concept of the segregation model of the gettering process was extended to explain the existence of an optimum annealing time.

2. Samples preparation and measurements

N-type, (100) oriented, 2.5–5 ohm·cm, CZ-grown silicon wafers were used in this experiment. The wafers were RCA cleaned. An oxidation at 1000°C in dry $O_2 + 2\%$ TCA ambient was performed to obtain 800 Å oxide thickness, followed by an annealing in N_2 at the same temperature for 30 min. It has been shown that this type of annealing reduces the oxidation stacking faults (OSFs) length [37] and improves the generation lifetime [38]. After that a backside phosphorus ion implantation with a dose of 10^{16} atoms/cm^{-2} and 120 KeV energy was performed. The segregation annealing was performed at $T = 900$°C in N_2. Different wafers were annealed for different time (0, 30, 60, 90, 120, and 150 min). From our previous experiments we have found that in the case of P ion implantation gettering the optimum segregation annealing temperature for maximum gettering efficiency is about 900°C. Similar results were reported in the literature [35].

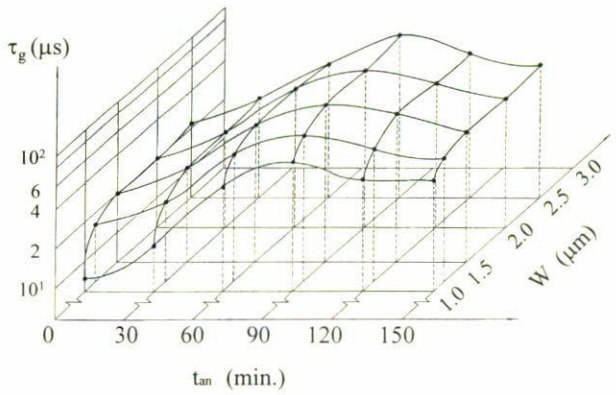

FIGURE 1. Quasi 3-dimensional representation of generation lifetime profile with the segregation annealing time as parameter.

Aluminum dots were evaporated through a metal mask on the top oxide. On the backside of the wafers, after removing the oxide, aluminum was also evaporated. The wafers were sintered in N_2/H_2 ambient at 425°C for 30 min.

The sine-voltage C-V method [35] was used to measure surface generation velocity and generation lifetime profile. The measurements were performed at 1 MHz, using BOONTON 72 B capacitance meter and WAVETEK 271 function generator was used as a voltage source.

3. Experimental results and discussion

Quasi 3-dimensional plot of generation lifetime with the segregation annealing time as parameter is shown in Fig. 1. The results show that the generation lifetime increases with the segregation annealing up to 90 min. For longer annealing times it decreases. On the other hand, in all samples the generation lifetime decreases towards the Si-SiO_2 interface. Another peculiarity is that the lower is the generation lifetime the larger is its increase, due to the segregation annealing, *i.e.*, the gettering efficiency is higher. It appears that the different process steps have affected the generation lifetime mostly in the near surface region.

The smaller values of τ_g observed near the Si-SiO_2 interface can be explained by the process of OSFs growth. It is well known that OSFs grow by releasing vacancies or absorbing Si self-interstitials from the surrounding matrix. The chemical driving force for the change of defect size, is given by [40]

$$F = \left(\frac{kT}{b^2}\right) \ln\left(\frac{C}{C_0}\right), \qquad (1)$$

where k is the Boltzmann's constant, T is the temperature, b is the Burgers vector, C is the vacancy concentration in equilibrium with the defect and C_0 is the equilibrium vacancy concentration in a defect free crystal. Factors opposing to the chemical driving force are the linear dislocation energy and the energy of the stacking faults. During the oxidation there is

a volume expansion. Part of this volume expansion is accommodated by generation of Si self-interstitials at the Si-SiO_2 interface. Some of these self-interstitials can recombine at the oxidizing interface and the rest diffuse into the bulk [41, 42]. In this case $C > C_0$ or there is undersaturation of vacancies, and the chemical driving force will be greater than the force determined by the stacking fault energy and the dislocation linear energy. This will result in a growth of OSFs. The growth of OSFs proceeds along the surface and into the bulk. Since the concentration of the Si self-interstitials decreases with the distance from the interface the density and the size of OSFs also decreases. Thus, the variation of τ_g near the Si-SiO_2 interface can be due to the spatial distribution of OSFs there. These defects are preferential sites of metallic impurities.

Several factors can be responsible for such behavior of generation lifetime as a function of segregation annealing time. From a physical point of view the process of gettering consists of three steps. According to the concept of the gettering process defects, especially metallic impurities, must be released from their original sites, diffuse to the implanted damaged region and be captured at the gettering sites. One of the three steps of gettering (release, diffusion or capture) will be the rate-limiting step for the gettering. For an optimum and constant temperature, segregation annealing time (diffusion) will be the rate-limiting step that controls gettering efficiency. In our case, in concordance with the above mechanism, one of the factors responsible to the increase of τ_g with the annealing time is the gettering of impurities. Such behavior of τ_g with the annealing time supports the combined segregation-extended defects model of the gettering process [35].

On the other hand, during annealing in neutral ambient there is Si self-interstitial undersaturation [43], *i.e.* $C < C_0$ and according to Eq. (1) the OSFs length will decrease. Therefore, another factor responsible for the increase of generation lifetime with the segregation annealing could be the decrease of OSFs length.

Several competing factors can be responsible for the behavior of τ_g with the segregation annealing in the range 90-150 min. It is clear that the shrinkage of the OSFs will continue. On the other hand, it is known [44] that dislocation loops lying on (111) planes edge dislocations and also dipoles lying parallel to $\langle 110 \rangle$ direction appear after annealing. The dislocation loops increase in size with anneal temperature up to 800°C. At this temperature apparently the loops stabilize, and do not change their size at higher annealing temperatures. However, for long annealing time the total density of dislocation decreases. The annihilation of defects is enhanced when they are decorated with impurities [40].

Using our experimental results and these ones from the literature [40, 41], we will extend the concept of the segregation-extended defects model of gettering [35] to include the process of metallic impurities release from the gettering sites for long annealing time. According to this model, the solubility of metallic impurities in the implanted region of high dislocation densities is given by

$$N_{mi,d} = N_d \exp\left(\frac{-E_{a,d}}{kT}\right), \tag{2}$$

where N_d is a preexponential factor which is a function of temperature and is related to the concentration of metallic impurities dissolved in the region of high dislocation densities and thus depends on the dislocation density. $E_{a,d}$ is the activation energy.

The solubility of metallic impurities in intrinsic or lightly doped Si is given by

$$N_{mi,i} = N_{\mathrm{Si}} \exp\left(\frac{-E_{a,i}}{kT}\right), \tag{3}$$

where N_{Si} is the number of Si atoms per unit volume and $E_{a,i}$ is the activation energy. The total solubility of metallic impurities in both regions is the sum of Eqs. (2) and (3)

$$\begin{aligned} N_{mi.T} &= N_{mi,d} + N_{mi,i} \\ &= N_d \exp\left(\frac{-E_{a,d}}{kT}\right) + N_{\mathrm{Si}} \exp\left(\frac{-E_{a,i}}{kT}\right). \end{aligned} \tag{4}$$

The segregation coefficient of metallic impurities between P implanted and lightly doped Si is defined as

$$K = \frac{N_{mi,T}}{N_{mi,i}} = 1 + \left(\frac{N_d}{N_{si}}\right) \exp\left[\frac{(E_{a,i} - E_{a,d})}{kT}\right]. \tag{5}$$

At a given temperature the segregation coefficient K is a constant which will determine the ratio of equilibrium concentration of metallic impurities in the region of high dislocation density to that in the lightly doped silicon. This means that the higher is K the higher is the gettering efficiency. Therefore, according to Eq. (5), the dislocation density should be as high as possible and the segregation annealing temperature should be as low as possible for high K. With the increase of annealing time dislocation density, N_d, decreases and according to Eq. (5) K also decreases. This requires release and redistribution of metallic impurities until a new equilibrium distribution between the implanted damaged region and the rest of the wafer is reached, corresponding to a new value of K. If so, then the generation lifetime must decrease, which coincides with our experimental results. This model explains also the physical meaning of the optimum annealing time. However, as it will be shown latter, other factors can also influence on the optimum annealing time.

Another factor, responsible for the degradation of τ_g in this annealing time interval, could be a metallic impurity contamination from the furnace. Indeed, looking at Fig. 1, it can be seen that the annealing times longer than 90 min have affected τ_g, especially in the near surface region. Here, it must be said that separate experiments have shown that for long annealing times there is a metallic impurity contamination from the furnace. A decrease of generation lifetime due to metallic impurity contamination from the furnace was also reported by Manchada *et al.* [45]. It is evident that the influence of the last two processes on the generation lifetime will compete

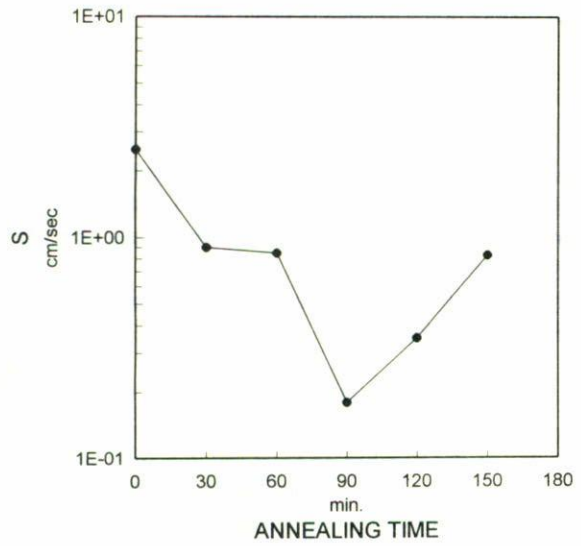

FIGURE 2. Surface generation velocity as a function of the segregation annealing time.

with that of the OSFs shrinkage. This fact can explain the slow decrease of τ_g for segregation annealing times longer than 90 min.

Surface generation velocity, S, as a function of the annealing time is presented at Fig. 2. It is seen from Fig. 2 that S decreases with the annealing time up to 90 min, and after that, decreases. It can be supposed that the gettering process, responsible for the gettering of impurities in the near surface region, also getters impurities from the Si-SiO_2 interface. The increase of S for longer annealing times can only be explained by a metallic impurity contamination from the furnace and not by the ion damage anneal.

4. Conclusions

Surface and bulk generation properties of MOS structures, gettered by P ion implantation, have been investigated. The parameter of the gettering was the segregation annealing time. It has been shown that the measurement of the generation lifetime depth profile and its quasi 3-dimensional representation offers easier identification of the factors controlling the generation lifetime, and better understanding the influence of the different process steps.

It has been found that τ_g increases with the distance from the Si-SiO_2 interface. On the other hand, the generation lifetime increases with the segregation annealing time up to the optimum annealing time, that was found to be 90 min in the present case. For longer annealing time than the optimum one the τ_g decreases.

The variation of τ_g near the Si-SiO_2 interface is explained by the model of OSFs growth. According to this model the size and the density of OSFs decreases with the distance from the interface and, hence, τ_g increases. The increase of τ_g with the segregation annealing time is due to the decrease of the OSFs size but mainly due to the gettering of metallic impurities.

To explain the τ_g behavior with annealing times longer than the optimum annealing time the concept of the segregation model of gettering was extended to include the annealing of dislocations and the subsequent release of metallic impurities from the gettering sites.

Three factors were identified to govern the behavior of τ_g for long annealing times. The first factor, according to the above model, is the decrease in the amount of disorder in the implanted region, the release of part of the metallic impurities trapped there and its redistribution in the wafer. The second factor is the shrinkage of OSFs due to the annealing in neutral ambient. The third factor is metallic impurity contamination from the furnace. The first and the third factors, which play a dominant role, compete with the second factor. These three factors determine the optimum annealing time necessary for maximum gettering efficiency.

The Si-SiO_2 interface is also affected by the gettering. Surface generation velocity decreases with the segregation annealing. However, it decreases for times longer than the optimum annealing time. This last fact confirms that there is a contamination from the furnace.

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