A simple procedure to design Glitch-less switched-current cells

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The description of non-idealities in Cascode Switched-Current (SI) cell as well as its application in analog signal processing is described. A test chip (CMOS, 1.5μm, N-well, 0-5 V) was designed to verify that the proposed method works successfully in the magnitude glitch reduction problem.

Keywords: Integrated circuits

Se describen las no idealidades de una celda *cascode* en corriente conmutada, así como su aplicación en procesamiento analógico de señales. Para ello, se fabricó un *chip* de prueba en tecnología CMOS para verificar el método propuesto para minimizar la magnitud de la respuesta espuria que aparece debido al proceso de conmutación aplicado.

Descriptores: Circuitos integrados

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1. Introduction

Recently the SI approach has been a field of research widely developed for the design of Mixed-Mode CMOS integrated systems. In this design option the basic building block is the Current Mirror (CM,) which requires minimum area to be integrated. Using minimum area allows the designer the possibility of high integration using a standard digital CMOS fabrication process. Furthermore, the SI technique can be used for designing mixed-mode system in which the possibility of the system malfunction, due the digital noise, can be avoided using the so-called cascode current mirror (CCM). A CCM has advantages such as its popularity in low voltage signal processing and A/D conversion because stray-inductance effects are less severe in SI designs than stray-capacitive effects in SC (Switched-capacitors) designs. Thus, SI circuits are excellent candidates for I/O design since a CCM is characterized by extremely low input impedance. However, SI circuits suffers of additional non-idealities because analog switches are required by the system to be designed. In that sense, several authors have been designed techniques to reduce glitches using the so-called dummy transistors (DT) [1], transmission gates (TG) [2] and a combination of both DT and TG [3]. Since the magnitude of glitches has not been successfully minimized up to now it is important to say that not all nodes are suitable to apply the techniques mentioned above. Thus, an analysis of resulting glitches in SI circuits and the use of suitable compensation scheme are presented in this letter. Finally, a test chip was designed to verify the validity of the proposed magnitud glitch-reduction technique.

2. The high-swing cascode current-mirror

As Fig. 1 shows the CCM has an input impedance of the order of $Z_{in} \approx 1/g_{mn}$ while the output impedance is given by Eq. (1), where g_{mn} and g_{ds} are the transconductance and conductance of the MOS transistor, respectively. It is easy to demonstrate that the minimum output voltage, V_x, is just $2V_{DSAT}$ and to take advantage of the high output impedance it is recommended to develop a cascode PMOS load transistors.

$$Z_{out} = \frac{g_{mn}}{g_{ds}^2}. \tag{1}$$

The Eq. (1) assumes that each transistor operates in its saturation region. The Fig. 2 shows the basic SI memory cell (or SI current branch) that uses a clocking scheme to process an input signal as an equivalent CCM. As an example, for Φ_1="**1**" (Φ_2="**0**"), the input resulting impedance is of the order of $1/g_{mn}$ which is equivalent to the CCM input branch. On the another hand, when Φ_1="**0**" (Φ_2="**1**") the equivalent impedance is given by Eq. (1). Using this switched design the bias current is reduced 50% respect the given one by the conventional CCM (see Fig. 1).

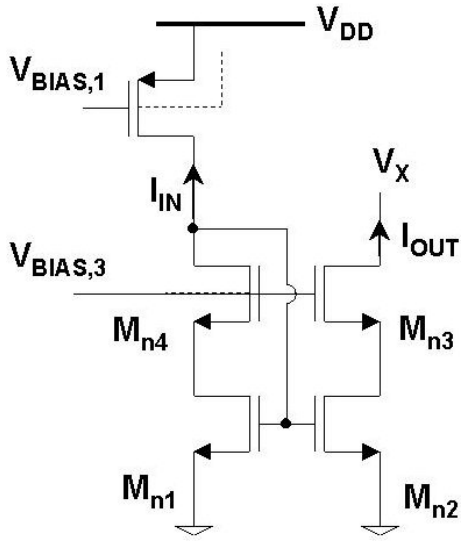

FIGURE 1 The advantage of using a cascode current mirrorallows the designer to develop complex systems just cascading basic cells. It is easy to demonstrate that the impedance ratio, defined as Z_{in}/Z_{out}, is lower than 0.01% that is a recommended value for analogue signal processing.

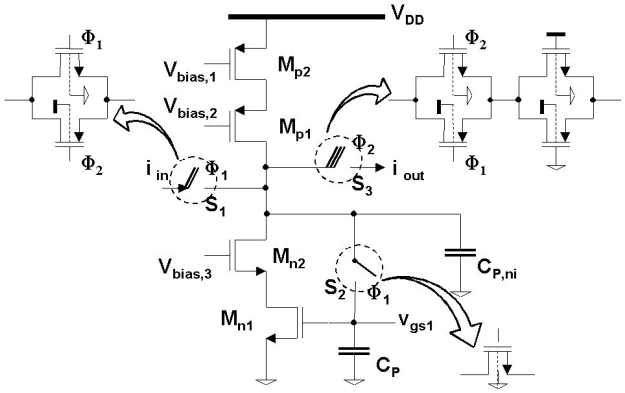

FIGURE 2 Basic switched-current cell suitable for describing clockfeedthrough. In this work all switches have minimum size (1.8μm/1.8μm).

3. Clockfeedthrough Analysis

Figure 2 shows a simple switched-current branch, which process the input signal i_{in} as an equivalent high-swing cascode current-mirror. Since the voltage v_{gs1} suffers a variation Δv_{gs1} due non-idealities it is important to consider, as a first analysis step, the situation in which the applied current is i_{in}=0. When switch S_2 is turned-on the total charge concentrated in the gate of M_{n1} is Q', however, when the clock signal V_Φ is falling down switch S_2 reaches its turn-off state and assuming there is no charge injection into C_p the voltage at the gate of M_{n1} is given by

$$v_{g1}\frac{C_p}{C_p+C_{ov}} = v'_{gs1} - V_\Phi\frac{C_{ov}}{C_p+C_{ov}} \qquad (2)$$

where C_p is a parasitic and C_{ov} is the overlap capacitance given by the gate and drain of S_2. Because M_{n1} operates in the saturation region, the value of C_p is approximately $2A_{n1}C'_{ox}/3$, where A_{n1} is the effective gate area of M_{n1} and C'_{ox} is the oxide capacitance per unit area. Another parasitic is the overlap capacitance C_{ov} that is due the lateral diffusion L_D of drain and source regions, this parasitic has a value given by $(W_{s2}L_D)C'_{ox}$. Thus, it is recommended to use minimum size for S_2 because the resulting math model for Δv_{gs1} can be described by

$$\left|\Delta v'_{gs1}\right| \approx V_\Phi\frac{3}{2}\cdot\frac{W_{s2}L_D}{W_{n1}(L_{n1}-2L_D)} \qquad (3)$$

Equation (3) shows two important facts: first, when $A_{n1} > W_{s1}L_D$ the error $\Delta v'_{gs1}$ tends toward its reduction and it is possible to approximate the area of M_{n1} as $(WL)_{n1}$ since the effect of L_D into A_{n1} is also minimized. Secondly, it is possible to use variable amplitude for V_Φ, however, that choice has to be analyzed carefully because the swing of the analog input signals could be reduced and this fact is not a good option in analog signal processing. On the other hand, the charge injection effect is caused by the charge accumulated under the gate of S_2 when V_Φ is high. Once V_Φ is low S_2 is turned-off and that accumulated charge constitutes a carrier flux, which flows towards the drain and source regions of S_2. Thus, that undesirable stimuli affect the value of v_{gs1} and an additional voltage variation can be seen. When the switching transistor S_2 turns off, a fraction of its channel charge Q_{ch} moves to the parasitic $C_{p,ni}$. The charge accumulated in C_p can be written as

$$Q_g = Q_{ch}\frac{C_p}{C_p+C_{p,ni}}; \qquad (4)$$

thus, the $v"_{gs1}$ variation due to the charge pumped effect is given by

$$v"_{gs1} = C_{ox}A_{sw}\frac{V_\Phi - V_T}{Cp+C_{p,ni}} \qquad (5)$$

where A_{sw} is the effective gate area of switch S_2. If the capacitance C_p is higher than $C_{p,n1}$ the total error

$$(v"_{gs1} + |\Delta v'_{gs1}|)$$

can be expressed as follows

$$\delta_{feedthrough} \approx \frac{3}{2(WL)_{n1}} \times \left[W_{s2}L_DV_\Phi + (WL)_{s2}(V_\Phi - V_{Tn})\right]. \qquad (6)$$

This result shows clearly the role of the great area required for M_{n1}. Indeed, if a similar analysis is done for the input switch S_1 the conclusion will be that the capacitance $C_{p,ni}$ has to be higher than the overlap capacitance C_{ovi}. Thus, that result is an additional condition to maintain the validity of Eq. (6). Strictly speaking, the condition $C_{ovi} < C_{p,ni} < C_p$ must be satisfied. Since the overlap parasitics of M_{n1} do not satisfy the condition given above, the

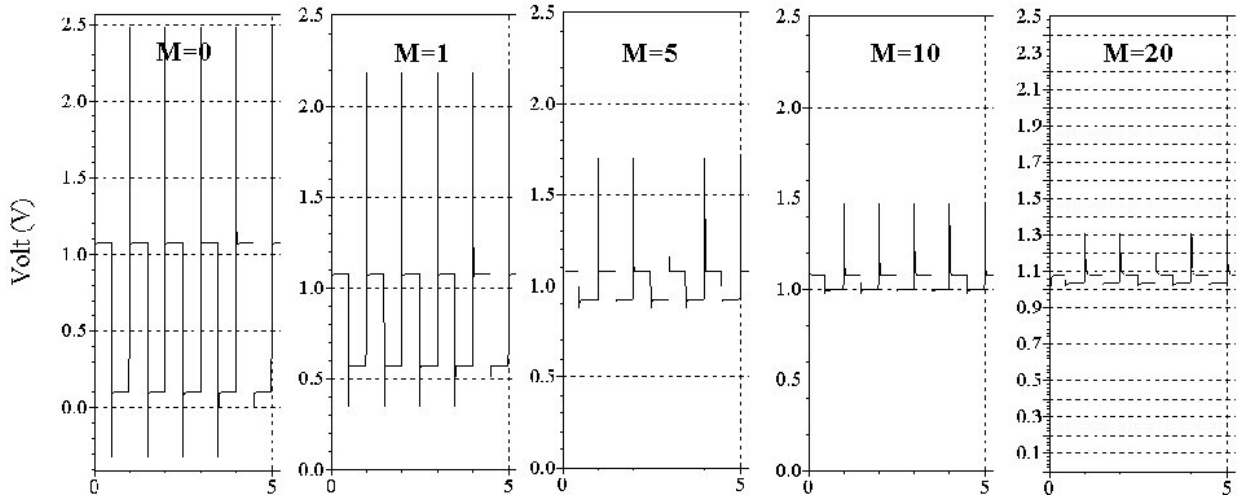

FIGURE 3 Tspice simulation result in which a NMOS capacitor has been designed with an area **M** times greater than M_{n1} area. The voltage variation $\delta_{feedthrough}$ was really decreased as area increases in value. The analysis was done using a sampling frequency of 1 MHz.

capacitance C_p can be implemented in several ways: 1) to use an NMOS transistor with source and drain shortened to ground (see Fig. 3). In this design option, the designer has control on the area of C_p and the validity of Eq. (6) is held; 2) to increase the size of M_{n1} in such a way that the magnitude of the glitches will be reduced to its minimum value.

The increment in size of M_{n1} was the option design used in this work and to reduce the resulting low-magnitude glitches the compensation switching MOS-array shown in Fig. 2 for each switch was used [4]. The size of the resulted transistors design are the following: $(33\mu m/27\mu m)_{p1}$, $(27/27)_{p2}$, $(81/16.2)_{n2}$, and $(86.4/16.2)_{n1.}$

4. Results

The facility used in this research was a 1.5μm CMOS process (N-well, 2 poly layers, 2 metals, 0-5 volts). The SI basic cell ($100x150\mu m^2$) drives a DC current I_{IN} of 10 μA. Cascading two SI basic cell and applying a feedback loop (from input node to output node) we obtain an inverter current integrator block, which can be used for the development of analog filter circuits. Since the processed analog signal has to be available any time the integrator includes an output current branch. Applying a 20kHz, 10μA square signal the experimental response of this cell is shown in Fig. 4a, and it can be seen that it operates in a successful way. Data were taken using the HP-Benchlink software.The result shows that the proposed circuit design reduced the feedthrough. Of course, a best performance can be seen when the DC current is increased, however, the purpose of the basic SI cell is to show its performance for a DC current of 10μA.

5. Conclusions

Because the required switching process produces spurious signals in all Switched-Current design, a compensation technique was proposed in this letter. The technique is economical and does not require a great integration area, which constitutes an important difference with the approaches given by other authors. The test of basic SI cells based in a high-swing cascode current-brach indicates that they operate in a successful way even for input signals of 10μA in amplitude.

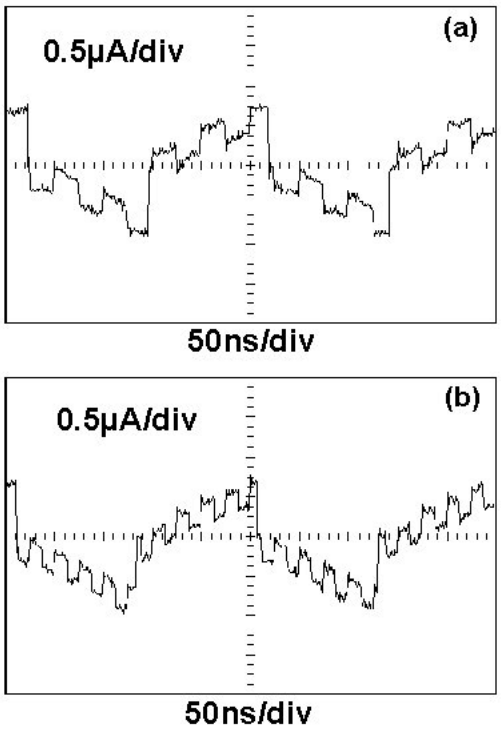

FIGURE 4 Experimental results for an inverter current integrator. In (a) a sampling frequency of 100 kHz was used, while in (b) the applied sampling frequency was of 200 kHz.

Acknowledgment

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