A CMOS transistor-only 2nd order low-pass ΣΔ modulator

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A simple procedure for designing a switched-current second-order ΣΔ modulator is presented. Since this design assumes a white noise spectrum due the quantization process, and by sizing the needed current branches according the proposed equivalent MOS transistor signal-to-noise ratio, a 2^{nd} order ΣΔ modulator suitable to develop an analog-to-digital converter for audio applications has been obtained. The experimental results verify in high percentage the utility of the proposed model. However, additional noise effects have to be taken into account to increase the performance of the modulator.

Keywords: Semiconductor devices; integrated circuits.

Se presenta un procedimiento simple para diseñar un modulador ΣΔ de segundo orden en corriente conmutada. En este diseño se asume que el ruido debido al proceso de cuantización presenta un espectro blanco, y dimensionando las ramas de corriente necesaria de acuerdo al modelo equivalente a nivel transistor propuesto para la razón señal-a-ruido, se obtiene un modulador ΣΔ de segundo orden adecuado para desarrollar un convertidor analógico-digital para aplicaciones de audio. Los resultados experimentales verifican en gran medida la utilidad del modelo, sin embargo, para incrementar el desempeño del modulador se deben tomar en cuenta efectos adicionales de ruido.

Descriptores: Dispositivos semiconductores; circuitos integrados.

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1. Introduction

Since last decade there is a research towards the development of analog signal processing based on the second-generation switched-current (SI) technique. The advantages of such a technique are that SI can be implemented in CMOS digital technologies and the building basic blocks are based in the current mirror, which requires low bias voltage for its operation. In practice, SI suffers of several non-idealities because of the switching process. In Ref. 1 a simple compensation technique was proposed to minimize the called clock-feedthrough (CFT) effect. In that work the authors have applied a modified MOS-switch that occupies low area and it reduces certainly in a high percentage the CFT. The experimental results of the proposed SI basic cells were published in Ref. 2 where the needed current branches were designed for driving a dc current of 10μA. Lately, a paper in which SI basic blocks for analog signal processing was published [3]. The basic blocks set includes the half/full delay cell as well as the inverter/non-inverter current integrator. As an example of such cells a SI biquadratic for designing a low-pass analog filter has been developed for audio applications [4]. Now, this paper presents the use of the basic cells described in Ref. 3 to design a SI ΣΔ modulator. The use of this circuit is for designing an analog-to-digital converter (ADC). Why an ADC? In mixed mode design it is desired to have analog sub-systems that are small in area and fully compatible with digital CMOS technology. Furthermore, it is well known that currently all communication systems process data in digital format, however, to have data in that format it is basic take into account a suitable translator. Additionally, a non-regular area for including the needed analog sub-system into a digital IC is an added constraint to the analog designer. As a consequence, to overcome the mentioned items, the design of an ADC is a suitable case of study for putting in practice the results obtained by our research group.

This paper is organized as follows: Section 2 shows basics on ΣΔ modulators as well as the design considerations using the SI approach. Experimental results are given in Sec. 3 where the modulator was designed according the design rules of a 1.2μm CMOS technology. Finally, in Sec. 4, a discussion of the experimental results and some conclusions are given.

2. Basics on ΣΔ

Assuming B_w is the signal bandwidth of a specific application, there are four needed steps to perform an analog-to-digital conversion:

- Antialias filtering. It is required to prevent folding into the baseband during the sampling process.
- Sampling. During this step a continuos-time signal x(t) is converted to a discrete-time signal x(nT), where **T** (usually named the sampling period) is inversely proportional to the sampling frequency $\mathbf{f}_s$, here **n** is an integer.
- Quantization. Each sampled continuos-amplitude signal corresponds to a signal that is discrete in time and amplitude.
- Encoding. In this step each discrete value supplying a digital signal just at the output of the ADC.

When the sampling frequency exceeds the Nyquist rate $\mathbf{f}_N$ it is possible to define the oversampling ratio as $\mathbf{M}=\mathbf{f}_s/\mathbf{f}_N$. To depict how oversampling works in the frequency domain, Fig. 1 shows the spectrum of the band-limited input signal and its corresponding spectrum after oversampling it with ratio **M**. According this, by using oversampling the anti-alias filtering is not yet a needed requirement. From the point of view of the analog IC designer, this fact means an important integration area reduction.

2.1. Description of the ΣΔ modulator

Since the application of the proposed design is for the audio range, the basic structure of a Low-Pass Second-Order ΣΔ modulator is illustrated in Fig. 2. It consists of two integrators, a quantizer, as well as two 1-bit Digital-to Analog converters (DAC). By looking at the structure of the ΣΔ modulator we know that SI circuits can be used for substituting each depicted block.

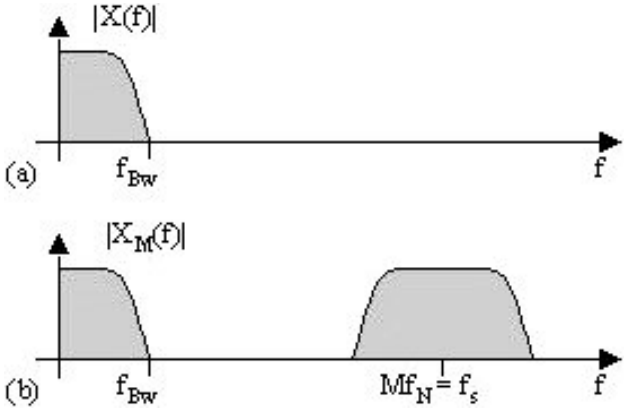

FIGURE 1. The band-limited signal-spectrum (a), and its signal-spectrum after oversampling (b). Here the applied sampling was M-times the Nyquist-rate.

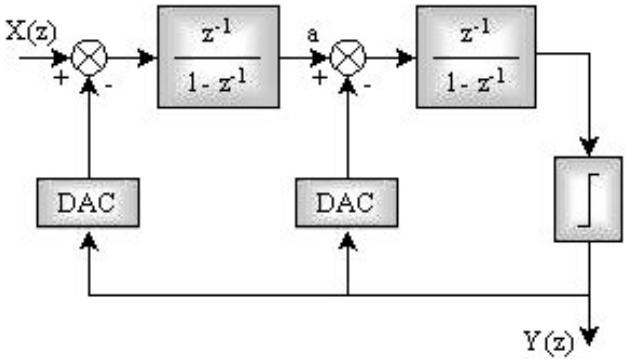

FIGURE 2. ΣΔ modulator. A second order design is recommended because the quantization noise is not correlated.

In the SI approach, the memory cell is the fundamental building block. As it is well known the memory cell must be a cascode current branch with added switches [2]. Such an array compensates in its entirely the majority of the switching process non-idealities [1]. This fact is a fundamental characteristic of the memory cell because reducing these non-idealities the ΣΔ modulator increases its performance. The current integrator is obtained once a unitary feedback loop is applied to the full-delay circuit that is obtained by cascading simply two memory cells. As far as this circuit is feedback connected the resulting integrator presents a redundant parallel switch connection since each one operate with complementary clocking scheme. This is the reason why the integrator shown in Fig. 3 requires just three switches. Furthermore, a continuos-time output current branch has been included to measure the current integrator response, which was designed for producing a modulator's gain of **a**=1/2.

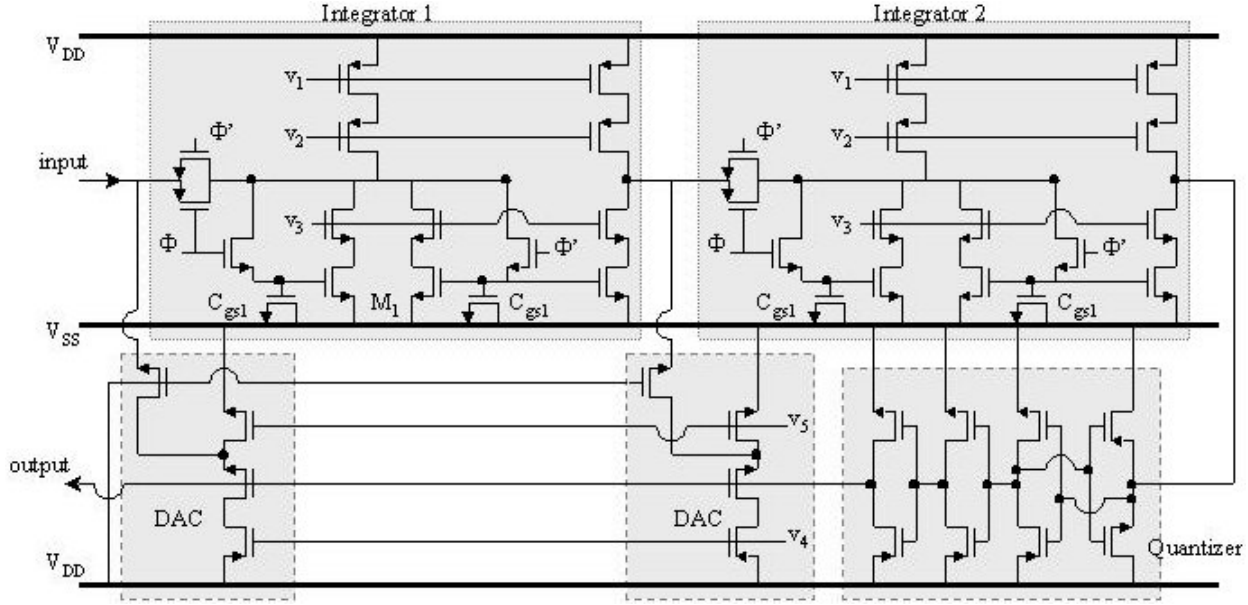

FIGURE 3. Schematic of the ΣΔ modulator. Since switched-current techniques offer full compatibility with digital CMOS technology, the capacitance C_{gs1} is a MOS transistor instead a double-poly capacitor.

It is well known that the signal-to-Noise ratio (SNR) for an **N**-th order $\Sigma\Delta$ modulator is given by

$$SNR = \frac{3}{2} \cdot \frac{2N+1}{\pi^{2N}} \cdot M^{2N+1}, \quad (1)$$

which is defined as the ratio of the power of a full-scale sinusoidal signal to the in-band quantization noise power. This equation assumes that the quantization error **e** is modeled as white noise having equal probability of laying anywhere in the range $\pm\Delta/2$, where Δ is the quantization step size.

As Eq. (1) indicates by increasing the modulator order the SNR improves its value. However, modulators with more than two integrators in the forward path exhibit instability. On the other hand, if **M** is equal to 2^r, where **r** is the doubling factor of the oversampling ratio, the SNR can be expressed as a function of the number equivalent of bits

$$SNR|_{N=2} \approx 2.5r - 2. \quad (2)$$

As described before, Eq. (1) shows that the SNR, and hence the number equivalent of bits in (2), increases for high values of **r**. Taken into account the entire audio frequency range, the number of needed bits for processing data can be from 12bits up to 14bits (equivalently 72-84dB). Therefore, the deduced doubling factor is 6.4, which has been rounded off in this work to **r**=7.

2.2. The CMOS SI Design

The simplified circuit diagram of the modulator is illustrated in Fig. 3, where Φ and Φ' are complementary clock phases. Here, the quantizer was implemented by means of a high-speed current comparator and the 1-bit DAC was simply designed using current sources controlled by the modulator output pulses. By assuming a sinusoidal input current with a full-scale power of $\Delta^2/8$, the SNR of the Low-Pass Second-Order $\Sigma\Delta$ modulator can be approximated according the following equation:

$$SNR = 10\log\left(\frac{15M}{2\left(\frac{\pi}{M}\right)^4 + 640 m_{th} kT \frac{(1+A)}{C_{gs1}(V_{gs}-V_{tn})^2_{M1}}}\right), \quad (3)$$

where $\mathbf{C}_{gs1}$ and $(V_{gs}\text{-}V_{tn})^2_{M1}$ are the gate-to-source capacitance and the first order approximation of the saturation voltage of memory transistor M_1, respectively. While $\mathbf{m}_{th}$ is a constant of the fabrication process between 1 and 2.5, **k** is the Boltzmann constant, **T** is the absolute temperature and **A** is the transconductance rate defined by g_{mn}/g_{mp}, where **n** (**p**) indicates the transconductance of the NMOS (PMOS) transistor. Equation (3) shows how important is the C_{gs} value. A high value of it not only increases the SNR of the $\Sigma\Delta$ modulator but also reduces the magnitude of glitches due clocking [2]. In practice, as the $\Sigma\Delta$ modulator is designed with the rules of a CMOS fabrication process, the capacitance C_{gs} is actually a MOS transistor with its drain and source shortened to V_{SS} (see Fig. 3). Additionally, (3) considers the following assumptions

- Thermal noise due the first integrator is reduced because $(V_{gs}\text{-}V_{tn})^2_{M1}$ represents a moderate bias voltage.
- The second integrator contributes only marginally to the total noise of the modulator.
- The voltages for biasing the current branches are stable voltage sources.

Using the design directions given by (3), and considering that the SNR must be of the order of 84dB, it is simple to size the current integrator in order to reach both a bandwidth of 20kHz for the modulator and the needed resolution. Furthermore, an oversampling ratio of **M**=2^7=128 and a capacitor C_{gs}=1.0 pF were proposed. The transistor used as the hold capacitor C_{gs} required the greatest integration area (W/L=131.4μm/6.0μm). Therefore the capacitor C_{gs1} was designed in the so-called finger array.

3. Results

To verify the validity of Eq. (3), a test chip was fabricated in a 1.2μm CMOS process. The chip includes an internal clock generator and the $\Sigma\Delta$ modulator. The last one occupies 0.25×0.17mm^2 (without bounding pads) and consumed 4mW from a 5V supply (V_{DD}=-V_{SS}=2.5V).

For testing purposes, the test chip has been attached to a PCB. The input is applied using the HP331220A sinusoidal signal source with a resistor (for V/I conversion). The last one is series connected with a capacitor (for filtering DC components) and then to the input pin. The output bit streams were captured with the HP8593A data system. Once the output pulses were stored 2048 points FFT were applied [5].

The SNR versus input level curves, which were obtained in the 20kHz bandwidth, was measured by dividing the power of the signal over the power of the noise. As a consequence of the oversampling, the best SNR peak was 66dB for 5.12 MHz sampling frequency. In other words, the number of equivalent bits was 11. One bit least that the minimum quantity for processing audio signals.

Figure 4 shows the measured modulator output spectrum for a sinusoidal signal of -9dB input level and 10kHz frequency. The spikes-less out-of-band suggest that the quantization error is correctly white noise. However the constant noise floor in the baseband was slightly higher than expected. One of several possible explanations for the noise increase may be coupled noise through the PCB, which was not optimized for noise reduction. Another one could be digital switching noise that is added to sensitive nodes via the MOS Capacitor, C_{gs1}. Additionally, as Fig. 3 shown, each DAC

includes a dummy transistor from its output node to the current integrator input. These dummies reduce the magnitude of the spikes given by the DAC output node. In practice, such transistors operate as resistors, which contribute with thermal noise. By analyzing the $\Sigma\Delta$ modulator loop we can conclude that this modulator is more sensitive to noise or error sources at the first integrator input that of the second integrator. As a consequence, these factors correspond to the lost bits.

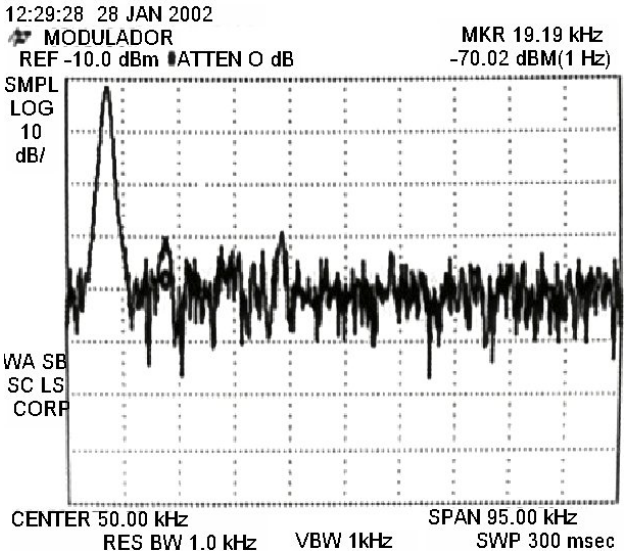

FIGURE 4. Measured modulator output spectrum for -10dB at 10kHz input signal when clocked at 5.12MHz.

However, our results are better than those reported early by several authors [6-8], which also have used the switched-current approach. Our design occupies the lowest integration area and it is useful for a wide frequency range.

4. Conclusions

A Switched-current second-order $\Sigma\Delta$ modulator has been designed and tested. It was fabricated in a CMOS 1.2μm, double-poly, double-metal technology. The circuit has been designed for developing an analog-to-digital converter for audio applications. Measurements show a SNR=66dB within a 20 kHz bandwidth, obtaining a resolution of 11 bits. Several factors are the reason why the design does not satisfy the original specifications. However, we can conclude that our design with tiny modifications allow us to reach more than the minimum number of bits for processing audio signals. Finally, it is important to mention that the equivalent MOS transistor SNR model, for designing a 2^{nd} order $\Sigma\Delta$ modulator [see Eq. (3)] is a useful design direction.

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