A noise tolerant technique for submicron dynamic digital circuits

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Signal integrity issues are a main concern in high performance circuits due to technological advancement. The smaller size of the CMOS transistors together with the increasing use of dynamic logic has brought signal integrity issues to the forefront. Hence it is necessary to develop noise-tolerant circuit techniques that will tolerate noise effects with slight performance penalties. In this paper a new noise tolerant dynamic digital circuit technique is proposed and demonstrated. Simulation results for CMOS AND gate show that the proposed technique has an improvement in the *ANTE* metric of 3.4x over conventional dynamic logic. A one-bit carry look-ahead adder implemented with the proposed technique has been designed and fabricated using an AMS 0.35μm CMOS N-well process. The experimental results show the noise immunity improvements of *ANTE* by 2.1x over the conventional dynamic circuit.

Keywords: Crosstalk; noise tolerance; CMOS integrated circuits.

Los avances de la tecnología de circuitos integrados CMOS de muy alta escala de integración VLSI (Very-Large Scale Integration) han permitido obtener microprocesadores rápidos y de bajo consumo de potencia aplicables a sistemas portátiles, inalámbricos y multimedia. La obtención de estos microprocesadores ha sido posible gracias al escalamiento de las dimensiones de los transistores y de sus interconexiones. Sin embargo, cuando los circuitos integrados se reducen (escalan), el ruido de acoplamiento entre las interconexiones degrada el desempeño de los sistemas. Debido a esto, es necesario desarrollar técnicas de tolerancia a ruido que reduzcan los efectos del ruido con mínima degradación de desempeño de los circuitos y sistemas. En este artículo se propone una nueva técnica de tolerancia al ruido de acoplamiento. Los resultados muestran que esta técnica mejora la robustez de los circuitos comparada con la obtenida con otras técnicas recientemente publicadas y consideradas de alta tolerancia al ruido de acoplamiento. La efectividad de la técnica propuesta es verificada mediante resultados experimentales obtenidos de un circuito sumador completo diseñado y fabricado utilizando una tecnología CMOS AMS de 0.35 μm.

Descriptores: Ruido de acoplamiento; tolerancia a ruido; circuitos integrados CMOS.

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1. Introduction

The rapid advancement of the VLSI circuit technology is driven by the increased use of portable and wireless systems with very low power budgets and the need for microprocessors with a faster operation speed. To achieve this, the dimensions of transistors and voltage supply are rapidly being scaled. However, technology scaling comes at the expense of some drawbacks. When the supply voltage is scaled, the threshold voltage of the devices also needs to be scaled to preserve the performance of the circuits, which implies an increase in leakage currents in the devices [1]. In addition, due to higher number of devices in a chip, more interconnections are used. These interconnections have a higher aspect ratios and are placed close to each other. Both the current interconnection design strategies and higher clock frequencies increase capacitive coupling effects in the interconnections. If a signal is launched through an interconnection, a noise pulse, also known as crosstalk, can be generated in a neighboring interconnection. The consequences are signal delays and logic failures, which in turn degrade the reliability of the systems. This problem is aggravated with the increased use of dynamic logic circuits, which have lower noise immunity than their static counterpart [2]. Hence, signal integrity issues are a main concern in high performance circuits.

New interconnect materials such as copper (Cu) and low-k dielectrics are used to alleviate the interconnect performance degradation. Cu, with its lower resistivity than aluminum (Al) and with its excellent electromigration resistance and relatively low cost, becomes a better choice than aluminum. Low-k dielectric materials reduce the parasitic capacitances between interconnections. Consequently, the combination of a low-k insulator and Cu will lead to performance improvement and cost reduction. However, some authors have argued that this solution alone may not be sufficient nor cost effective to solve the interconnection problem [3,4].

There are two design strategies to address interconnect noise issues:

1) reducing the peak noise pulse generated in the interconnections by means of interconnect optimization (repeater insertion, wire sizing, driver sizing, etc.), and
2) designing noise-tolerant circuits that will tolerate increasingly higher noise pulses appearing at their inputs. In this work, the second strategy is addressed.

In this paper a new noise-tolerant dynamic digital circuit is proposed and its feasibility is demonstrated by means of experimental results. The experimental results are derived from measurements on a designed and fabricated full-adder circuit implemented with the proposed technique. The rest of the paper is organized as follows: the origin of noise issues in deep submicron circuits is review in Sec. 2. The noise-immunity mechanisms, advantages and disadvantages of previous noise-tolerant techniques are discussed in Sec. 3. The structure and operation of the proposed technique, as well as its application to TSPC dynamic logic style are addressed in Sec. 4. The performance of the proposed technique is compared with other previously published techniques and with conventional logic in Sec. 5. Experimental results from a fabricated full-adder showing the improvement in noise-immunity of the proposed technique are presented in Sec. 6. Finally, the conclusions of the work are given in Sec. 7.

2. The noise problem

Two kinds of wires are distinguished with respect to wire delay under technology scaling [5]: local and global wires. Local wires are used to connect logic gates within blocks, and when transistors and blocks shrink, these wires scale. Global wires connect many blocks and usually span a significant part of a die. Due to increase in the density and size of the die, these wires actually become larger.

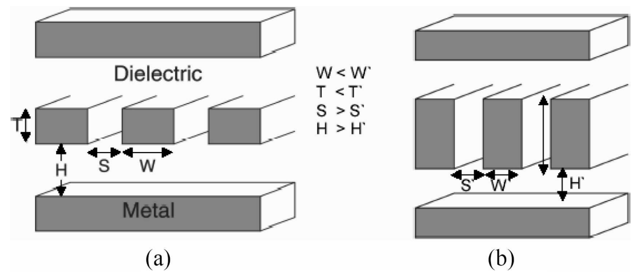
To maintain interconnect performance, global interconnects usually do not shrink or their dimensions are even increased at the same rate as the chip size. This is commonly known as reverse scaling. In the reverse scaling scheme, the resistance decreases and the capacitance grows, resulting in a constant RC delay at the expense of wire density. If global interconnects do not scale in length, the wire delay related to gate delay and the coupling capacitance between wires are increased.

As technologies scale, resistance in the local wires increases since the width and height both scale down. To avoid higher interconnect resistance, the aspect ratio of the interconnects is increased. This means that the vertical dimension of wires is being scaled more slowly compared to the horizontal dimension (see Fig. 1). However, due to the increased aspect ratio, the sidewall capacitance becomes an important part of the total capacitance in the interconnects [3,6].

The noise voltage induced between interconnects depends on both the coupling capacitance to total capacitance ratio as well as on the ratio of the strengths of the gates driving the two wires. A first-order model for this coupling noise is [5]

$$V_n = V_{dd}\left(\frac{C_{coupling}}{C_{total}}\right)\left(\frac{1}{1+\frac{\tau_{agg}}{\tau_{vic}}}\right) \quad (1)$$

where τ_{agg} and τ_{vic} are the time constants of the aggressor and victim drivers, respectively. As the ratio of the coupling capacitance to the total capacitance increases, and if the aggressor has a much smaller time constant than the victim



(a) (b)

FIGURE 1. The aspect ratio (T/W) increases and the proximity between the interconnections (S) lessens. (a) Current technologies, and (b) future technologies.

(and is hence much stronger), the noise approaches a worse case. With these trends, noise pulses of significant amplitude and width appear in current integrated circuits. These noise pulses can propagate and arrive at the inputs of logic gates. Consequently, the reliability of the circuits is degraded and logic failures may occur. Thus the need for high performance systems with increased noise tolerance is evident. Noise-tolerant circuit techniques that tolerate noise effects with slight performance penalties need to be designed. These noise-tolerant techniques are useful, especially in those parts of the systems where there is an increasing amount of data as in data-paths.

3. Previous noise tolerant techniques

There are in the literature many noise tolerant techniques [7]. Noise-tolerant techniques are classified into four main categories based on their principle of operation:

1) use of a keeper;
2) precharging internal nodes;
3) raising source voltage; and
4) constructing complementary p-network.

Many noise-tolerant techniques raise the noise threshold voltage (V_{nth}) of gates by increasing the source voltage of the transistors in the pull-down network (PDN) using the input data or the clock signal. V_{nth} is defined as the minimum input voltage required to cause a logic transition at the output. (Vnth is defined as the minimum input voltage required to cause a logic transition at the output). This precharge increases the threshold voltage of the NMOS transistors in the PDN, taking advantage of the body effect. Consequently, V_{nth} is also increased.

In this section a review of only two proposed noise-tolerant techniques is presented for space reasons.

The basic TSPC (True-Single Phase Clock) building block [2,12], is shown in Fig. 2a. This TSPC building block is implemented with Twin-transistor and Triple transistor techniques in Figs. 2b and 2c. The numbers beside the transistors indicate the transistor channel widths. The channel width for PMOS and NMOS transistors is referred to as the size of the transistor. All transistors have the same channel length (0.30μm).

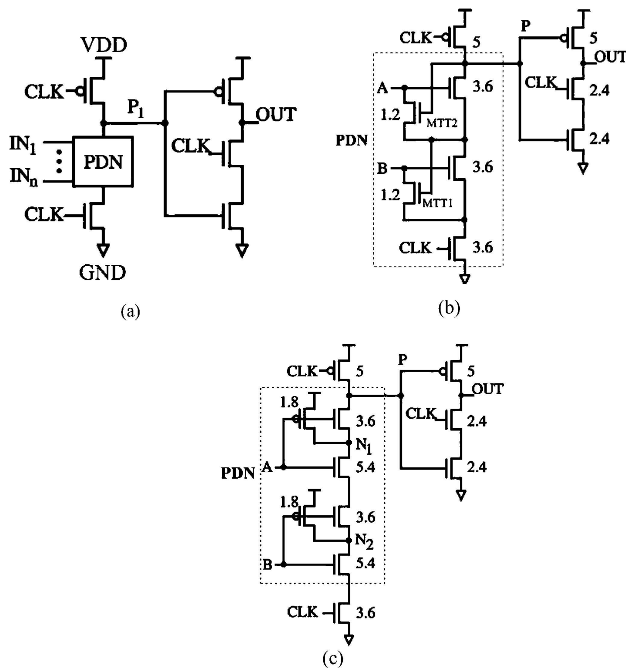


FIGURE 2. 2-input TSPC AND gates: (a) Conventional TSPC, (b) implemented with Twin-transistor technique, and (c) with Triple-transistor technique.

The **Twin-Transistor technique** [8], shown in Fig. 2b, rises the voltage of the N-logic PDN internal nodes via additional transistors M_{TTx}. Due to body-effect, the noise threshold voltage of the N-logic PDN transistors is increased. Hence, the tolerance of the gate is improved. The use of gate inputs to raise the voltage of the PDN internal nodes is one drawback because the load capacitance of the gate input drivers is increased. Furthermore, this technique cannot be applied to pipelined logic like TSPC because the inputs of n-type blocks are floating in the evaluation phase. Consider the case when this technique is applied to n-type blocks in a pipelined system. If all inputs of an n-type block are high at the beginning of the evaluation phase, the voltage level of the upper input is degraded by a charge redistribution mechanism. In this way, buffers between N- and P-blocks are needed to apply the Twin-transistor technique in TSPC logic. Fig. 2c shows the **Triple-Transistor technique** [9] implemented in a 2-input AND gate. In this technique, each NMOS transistor is replaced by three transistors in the PDN to improve the noise-tolerance. If during the evaluation phase all inputs are high, a voltage divider is formed by the PMOS and NMOS transistors at nodes N_1 and N_2. The noise tolerance is improved because the V_{th} of the AND gate equals the V_{th} of the static inverters that operate as voltage dividers; V_{th} can be adjusted modifying the transistor width to length ratios. One drawback of this technique is the significant delay penalty for AND gates due to the duplicated N-logic and the increased capacitance at the gate inputs. Power consumption penalty is increased because two transistors are added for each transistor in the original PDN.

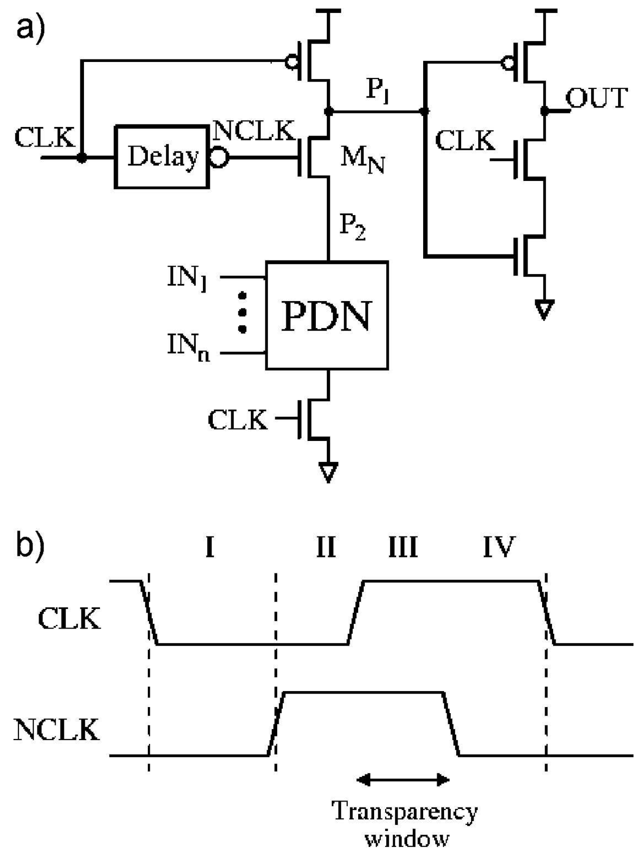


FIGURE 3. Proposed noise tolerant technique.

4. Proposed technique

In this section, a technique for improving noise tolerance of digital dynamic gates is proposed [10,11]. The operation and design constraints of the technique are stated. Then, the technique is applied to TSPC gates.

Figure 3 shows the block diagram and the timing diagram of a conventional TSPC precharge latch with proposed the noise-tolerant technique proposed. The PDN can be a simple transistor or a combination of AND-OR functions. In this way, a variety of logic functions can be constructed. Note that in Fig. 3a the PDN does not require modifications, *i.e.*, the inputs have not been used to precharge any internal node in the PDN. This is advantageous because the capacitive loads at the inputs remain the same.

4.1. Operation of the proposed technique

According to Fig. 3, on the falling edge of the clock signal (CLK) the circuit enters in the precharge phase, [stage I in Fig. 3b]. The dynamic node P_1 is precharged high, and the output (OUT) is isolated from the inputs holding its previous value. As noted in Fig. 3b, the NCLK signal is low in stage I. Consequently, the transistor M_N is OFF and the transistor M_P is turned ON. After a delay time following the beginning of the precharge phase, the NCLK signal goes high [stage II in Fig. 3b] turning ON the transistor M_N while the node P_2 is

precharged to V_{dd} through M_P transistor. On the rising edge of the clock, the circuit enters the evaluation phase where two stages are also distinguished. In stage III, the circuit is in the transparent mode and a transparency window is defined. The transistor M_P is turned OFF and the logic state of the OUT is determined by the state of the PDN. If the PDN is ON, the dynamic node P_1 is discharged and the OUT goes high. If the PDN is OFF, no *dc* path to ground is formed and the node P_1 remains high. Consequently, OUT goes low. In stage IV, NCLK goes low turning the transistor M_N OFF. As a consequence P_1 and OUT are isolated from the PDN during the rest of the evaluation phase.

4.2. Noise tolerance mechanism of the proposed technique

The performance of the proposed technique is analyzed in the presence of crosstalk noise (refer to Fig. 3). Let us assume that in the evaluation phase (CLK=1) all the inputs are HIGH except one in which a crosstalk pulse appears, turning the PDN momentarily ON. Then a direct path from P_1 to ground is generated. In this situation the proposed technique uses two mechanisms to increase the noise tolerance:

(1) The threshold voltage of the transistor M_N is increased due to body effect [12] because the node P_2 is precharged to V_{dd} prior to the evaluation phase. Consequently, the noise pulse at the inputs of the gate requires a larger amplitude to discharge the dynamic node P_1 and to generate a logic failure at the output. In this way, the noise immunity of the circuit is increased during the transparency window.

(2) NCLK goes low in the evaluation phase and the dynamic node P_1 is isolated from the PDN. The noise immunity is indeed improved because any noise influence at the circuit inputs is not reflected at node P_1 and at the output.

4.3. Design requirements of the transparency window

The width of the transparency window is the main design parameter to take into account because it determines the performance and the noise tolerance level of the circuits.

The transparency window width t_{tw}, (see Fig. 4) is defined by

$$t_{tw} = t_D^{\max} + \Delta t,$$

where $t_D^{\max}$ is the discharge time of the node P_1, determined by the stack of NMOS transistors formed by M_N, the PDN and the clocked transistor (see Fig. 3a). Δt is the time difference between the falling edge of the waveform at node P_1 and NCLK. This time is needed to assure a correct logic operation. The transparency window must be larger than the discharge time of node P_1, otherwise the precharge node P_1 does not discharge completely when the PDN is ON. If we make Δt very large, we can be sure that the gate will operate properly but at the expense of less noise immunity. During the transparency window the noise immunity is improved by precharging the internal node P_2. On the other hand, if Δt is very narrow, higher noise tolerance can be reached but the precharge node P_1 will not discharge completely. Hence, an incorrect logic level may appear at the output.

In this way, the trade-off between noise immunity and performance is determined by the transparency window width. Furthermore, the local generation of the NCLK signal by the delay circuitry allows better control of transparency window width, so that a sufficiently narrow transparency window can be produced and better noise tolerance can be achieved.

It is worth to mention that, even if Δt is narrow in such a way that P_1 does not discharge completely, the output voltage can still reach a logic level "1" with a slight delay penalty. Hence, with a careful design of the transparency window, higher noise tolerance can be achieved.

4.4. Application to TSPC AND gates

In TSPC logic style, the PDN can be replaced by any combination of NMOS transistors to embed logic functions into the latch. If the PDN is replaced by two series transistors in Fig. 3a, a 2-input TSPC AND gate implemented with the proposed noise-tolerant technique is constructed (see Fig. 5).

The delay circuitry can be constructed with three cascaded static inverters (see Fig. 5). The transparency window can be adjusted to meet the noise-immunity-performance requirements by a proper selection inverters strength in the delay circuitry. Precharge-evaluate logic has a single critical transition: the HIGH to LOW transition of the precharge node. Thus, the gates are optimized for speed in the evaluate direction [13]. Using HSPICE and parameters listed in Table I, several simulations were done to verify the operation of the proposed technique in TSPC AND gates.

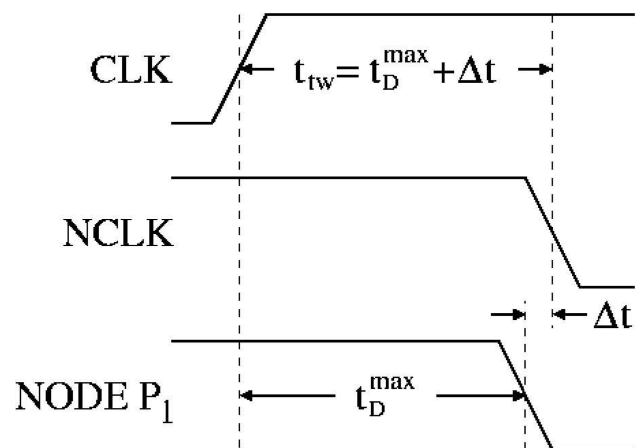


FIGURE 4. The delay time for the transparency window depends on the discharge time of the precharge P_1 node.

TABLE I. Simulation parameters.

Parameter	Description
Technology	0.35 μm AMS
Channel length	0.30 μm
Min. Gate width	0.6 μm
V_{tp}	-0.62 V
V_{tn}	0.46 V
V_{DD}	3.3 V
MOSFET Model	BSIM3v3
Data/Clock slopes of ideal signals	100 ps
Clock duty-cycle	50%
Delay calculation	Between 50% points
Clock frequency	1.5 GHz for latches, 1 GHz for gates

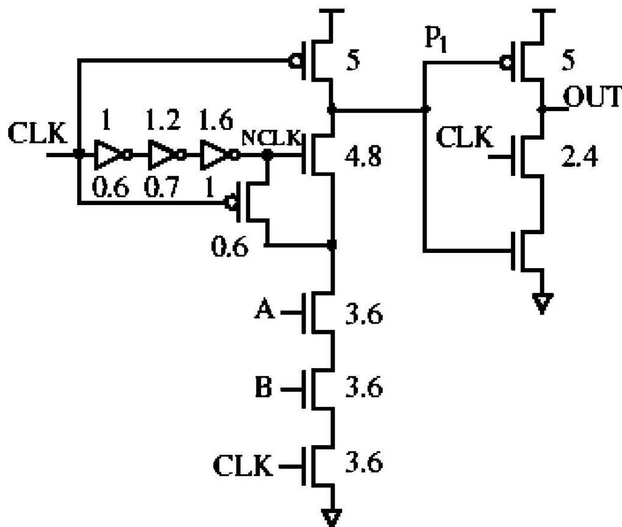


FIGURE 5. 2-input AND gate with the proposed noise-tolerant dynamic circuit technique.

The behavior of the 2-input TSPC AND gate implemented with the proposed technique is shown in Fig. 6. The signal NCLK is always delayed with respect to the CLK signal. When A and B are low (INPUT in Fig. 6), the precharge node P_1 remains at high logic level in the evaluation phase. As a consequence the OUT low. When A and B are high the precharge node P_1 goes low during the transparency window. Consequently, the OUT goes high.

5. Simulation results and comparisons

In this section, the performance of the proposed noise tolerant technique is compared with techniques proposed by other authors. Twin-transistor and Triple-transistor techniques are chosen for purposes of comparison. Conventional dynamic gates have also been considered. The parameters considered for comparison are:

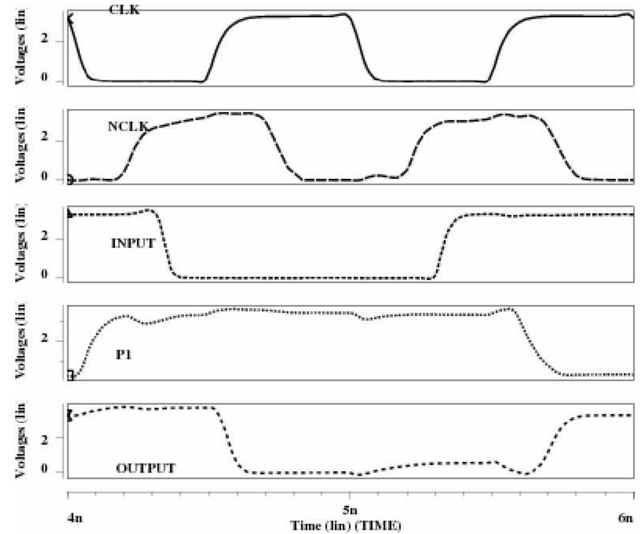


FIGURE 6. A transient analysis of a 2-input AND gate implemented with the proposed technique.

- *Noise tolerance.* Noise immunity curve [14], Average Noise Threshold Energy (ANTE) [15] and ANTE/delay are determined for the noise tolerant techniques.

- *Power consumption*. The average power consumption is measured for the whole circuit.

- *Delay.* The delay is measured at 50% points from the rising clock edge to the output.

Figures 2 and 5 show the schematic diagram of the 2-input AND gates used in the simulations, and the numbers beside the transistors indicate the transistor channel widths. Although Twin-transistor and Triple-transistor techniques were proposed for Domino circuits, they are used in TSPC circuits for purposes of comparison.

In Figs. 2 and 5 one input is tied to V_{dd} while a noise pulse is applied to the other. If the injected noise pulse has sufficient width and amplitude, - *i.e.*, energy -, it will be propagated through the output of the gate. The noise immunity curve is obtained as follows: The noise width is fixed while the noise amplitude is increased until the logic state of the load (P-latch) changes. The same procedure is repeated for different pulse widths until the noise immunity curve is constructed.

Figure 7 shows the resulting noise immunity curves for 2-input AND gates implemented with Twin-transistor, Triple-transistor conventional TSPC and the proposed technique. As can be seen, the proposed technique and Triple Transistor technique have comparable noise immunity. To figure out which one has the highest noise immunity, we use the Average Noise Threshold Energy metric (ANTE) [15]. It can be seen in Table II that the proposed technique has the highest ANTE. Moreover, delay measures indicate a delay penalty of 21.5% in the proposed technique as opposed to 73.8% in Triple-transistor technique and 10.5% for Twin-Transistor technique for AND gates.

TABLE II. Performance for 2-input TSPC AND gate.

Technique	Power (mW)	ANTE (V^2ps)	Delay (ps)	ANTE/Delay (V^2)
Conv. dynamic [2]	1.32	656	184.4	3.55
Twin-transistor [8]	1.40	1003	203.8	4.92
Triple transistor [9]	1.63	1858	320.6	5.79
Proposed technique	1.70	2227	224.2	9.93

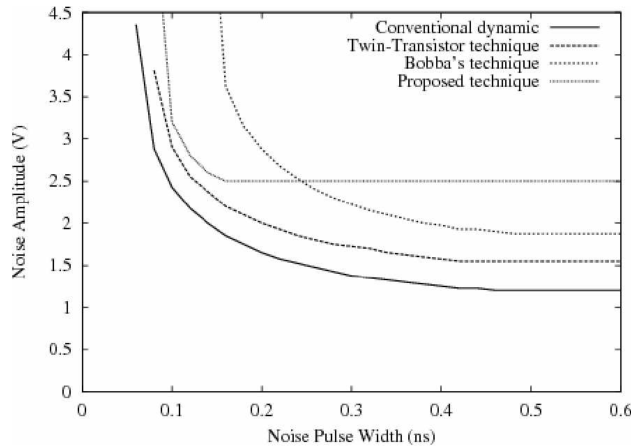


FIGURE 7. Noise immunity curves of AND gates.

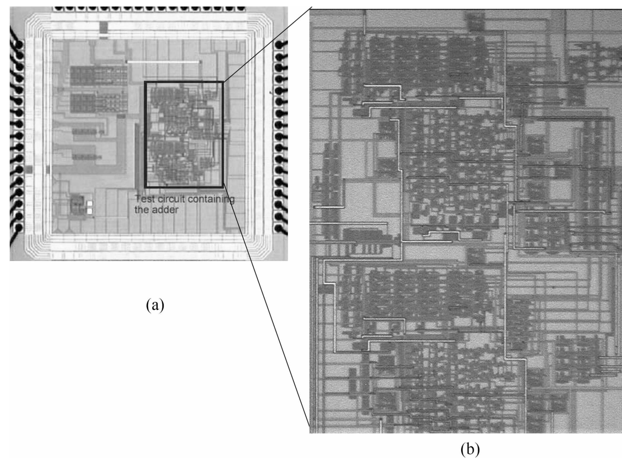


FIGURE 8. Photograph of the fabricated chip (a) full chip, (b) 1-bit carry look-ahead full adder.

All noise tolerant techniques increase the ANTE at the expense of increased delay, power consumption or area. Hence, the main aim of noise-tolerant techniques is to increase noise tolerance of a circuit with less performance degradation. The ratio ANTE/delay in Table II indicates the delay penalization incurred in improving noise immunity for the different techniques. The proposed technique has the highest ANTE-Delay ratio for AND gates. Another important characteristic of the proposed technique is the fact that, for wide noise pulses, the tolerated noise amplitude is higher than for the other techniques (see Fig. 7). This fact can be further exploited in future technologies because the peak noise value scales and noise pulse width increases with voltage scaling [8].

6. Experimental results

A one-bit carry look-ahead full adder implemented with the proposed technique has been designed and fabricated. A four-stage pipeline structure has been considered. TSPC dynamic logic is used for the adder with the proposed technique implemented in both the P and N blocks. AMS 0.35μm technology has been used. A photograph of the fabricated chip is shown in Fig. 8. Dices were packaged in a 68 pins JLCC package. The test circuit was fabricated together with others projects. The adder is the circuit located on the right-hand side of the photograph.

The logic diagram of the full adder is shown in Fig. 9. The node “a” located at the output of the first pipeline stage of the designed full adder (see Fig. 9a) has been selected as the victim node. By applying a noise pulse at this node, a realistic logic failure situation can be produced. This concept can be clarified using the full-adder logic diagram shown in Fig. 9. The noise pulse is injected at the node marked “a”. A noise pulse with sufficient amplitude and width will generate an undesirable logic transition at the output nodes marked “b” and “d”. This failure, depending on the input levels, will propagate through “c”, “f” or “e” and finally to the outputs “s_0” and “c_1”. In this way, both the N-blocks and the P-blocks are affected by the noise effects and help to measure the overall noise immunity.

Due to the random characteristic of crosstalk noise, it is difficult to control the generation and shape of noise pulses by means of intentional capacitive coupling between two or three interconnection lines. An easy way to generate glitches is to use a noise injection circuit (NIC) [8]. The purpose of the NIC is to generate noise pulses of certain amplitude and width to be applied at a selected victim node in the full adder. Fig. 10a shows the schematic diagram of the noise injection circuit, which has a tunable delay circuitry made of three inverters.

The propagation delay of the three inverter chain and hence the noise pulse width W_N is controlled by the voltage V_{NW}. This delay circuitry is connected to a two-input NAND gate. A pulse signal is applied to both the input of the delay circuitry and the NAND gate (node T). Consequently, a pulse with a controlled width is generated at node C (see Fig. 10b). The output stage of the NIC is an inverter whose supply voltage V_{NA} is tuned to control the amplitude of the noise pulse. When the NIC is triggered, the output inverter acts as a static CMOS inverter because the transistor M_g is ON. In absence of a pulse signal at the input of the NIC node, T is LOW and C is high. Thus the transistors M_g and M_p are OFF and consequently the output of the NIC is in a high-impedance state. In this state, the NIC does not interfere with the normal function of the full adder.

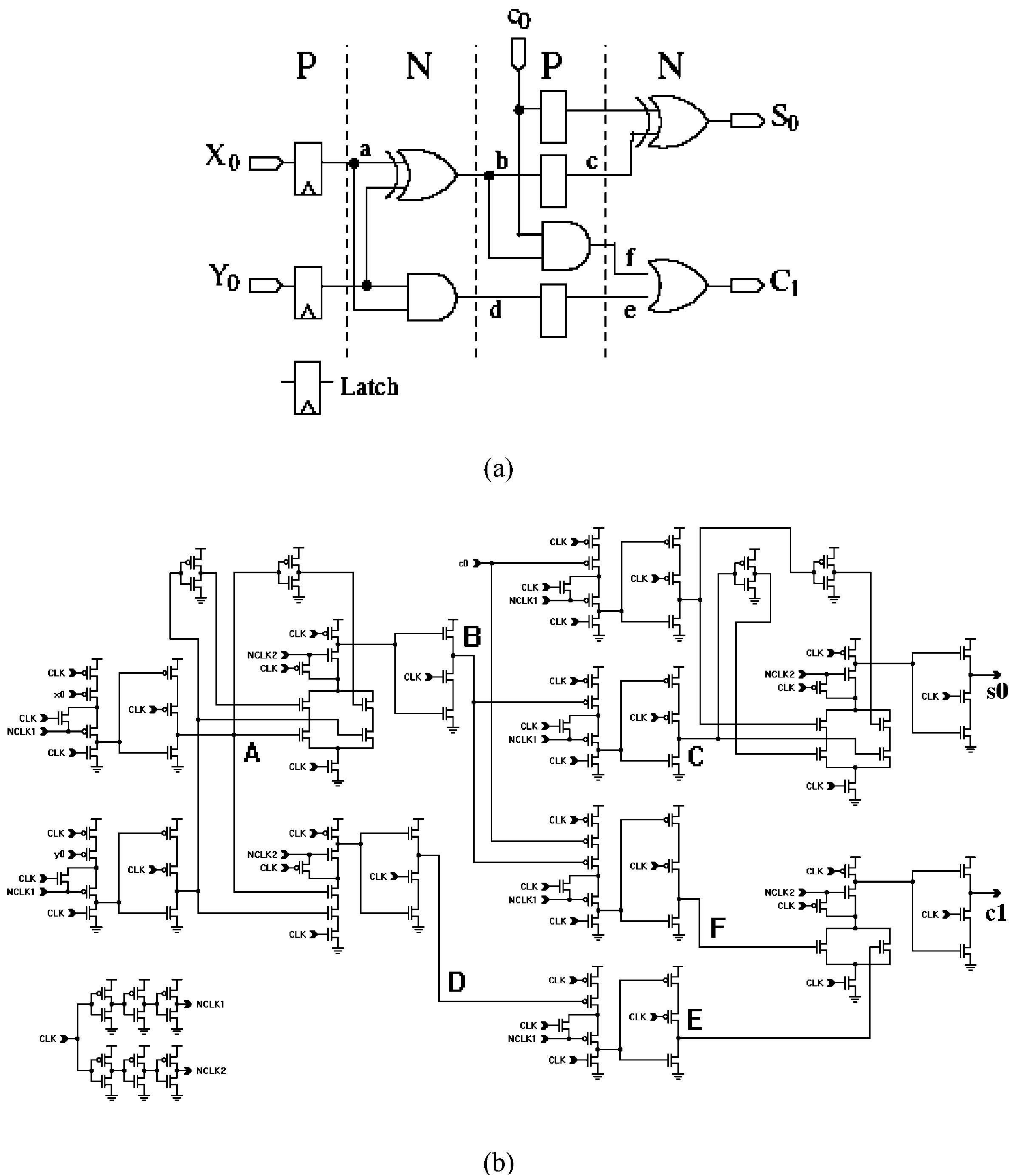


FIGURE 9. Logic (a) and schematic (b) diagram of the 1-bit carry look-ahead full adder.

6.1. Normal operation of the test circuit

In this section the time-domain operation of the full adder is shown with the NIC disabled. The signal waveforms are related to the full adder logic diagram shown in Fig. 9. X_0, Y_0 and C_0 are the inputs, and S_0 and C_1 are the outputs, sum and carry terms respectively. The clock frequency is f_{CLK}=100MHz and the supply voltage is V_{dd}=3.3V. Experimental results from a fabricated chip have been obtained. The input signals in Fig. 11a, marked X_0, Y_0 and C_0, are applied to the test circuit. The corresponding outputs S_0 and C_1, shown in Fig. 11b, have the same pulse pattern as that of the inputs because the test circuit is adding only inputs of the form “000” and “111”. As noted, the test circuit operates correctly.

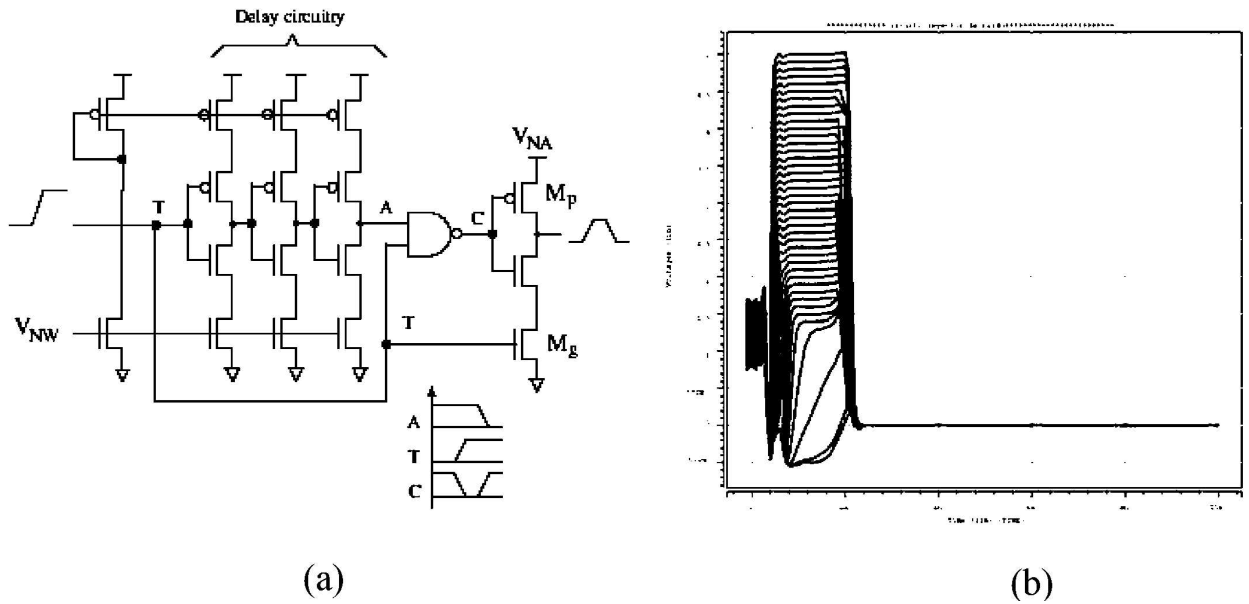


FIGURE 10. Diagram of the noise injection circuit. (a) Noise injection circuit, b) Noise pulses.

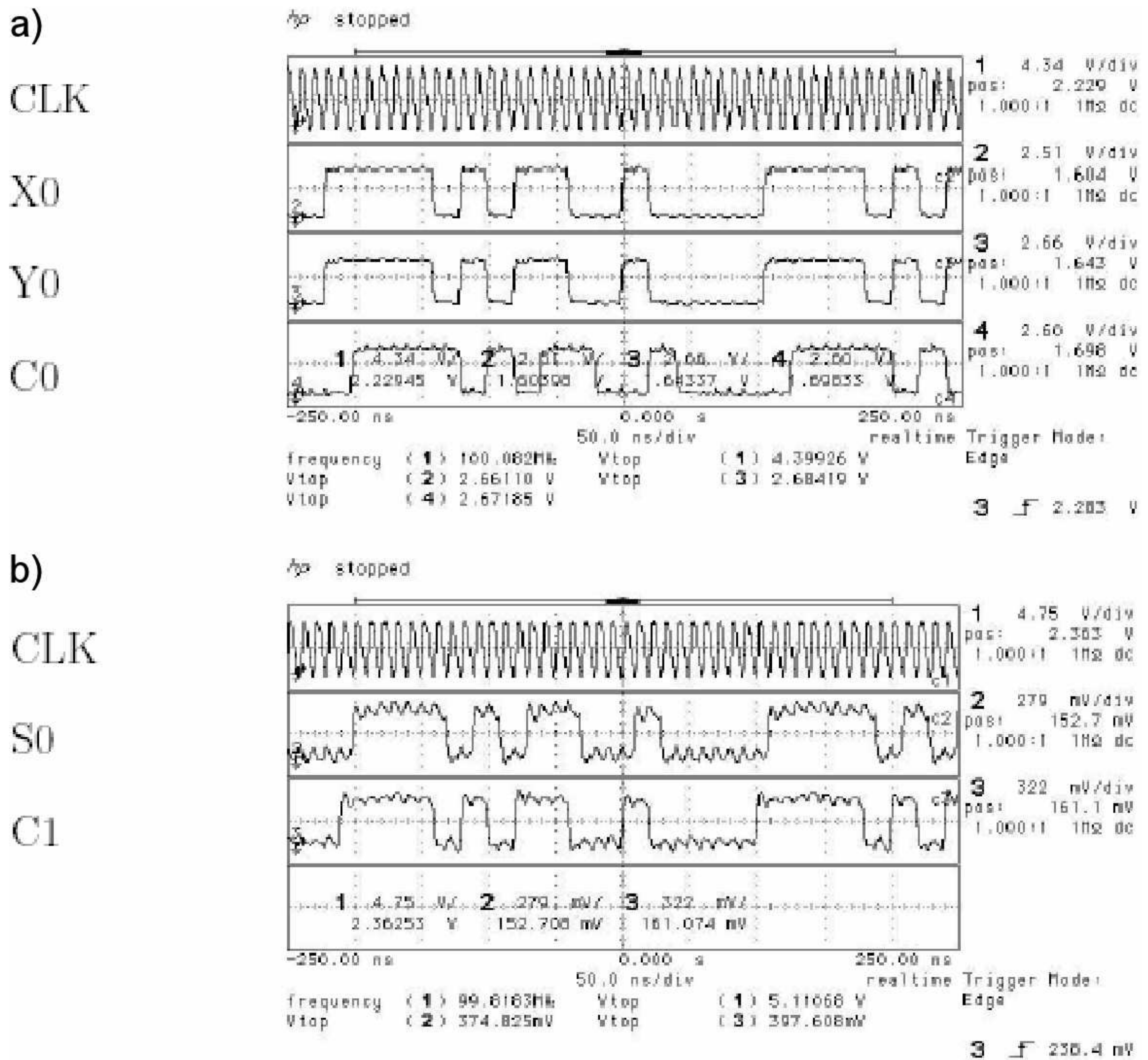


FIGURE 11. (a) Pseudo random input signals applied to the full adder, fCLK=100MHz, Vdd=3.3V, and (b) full adder outputs.

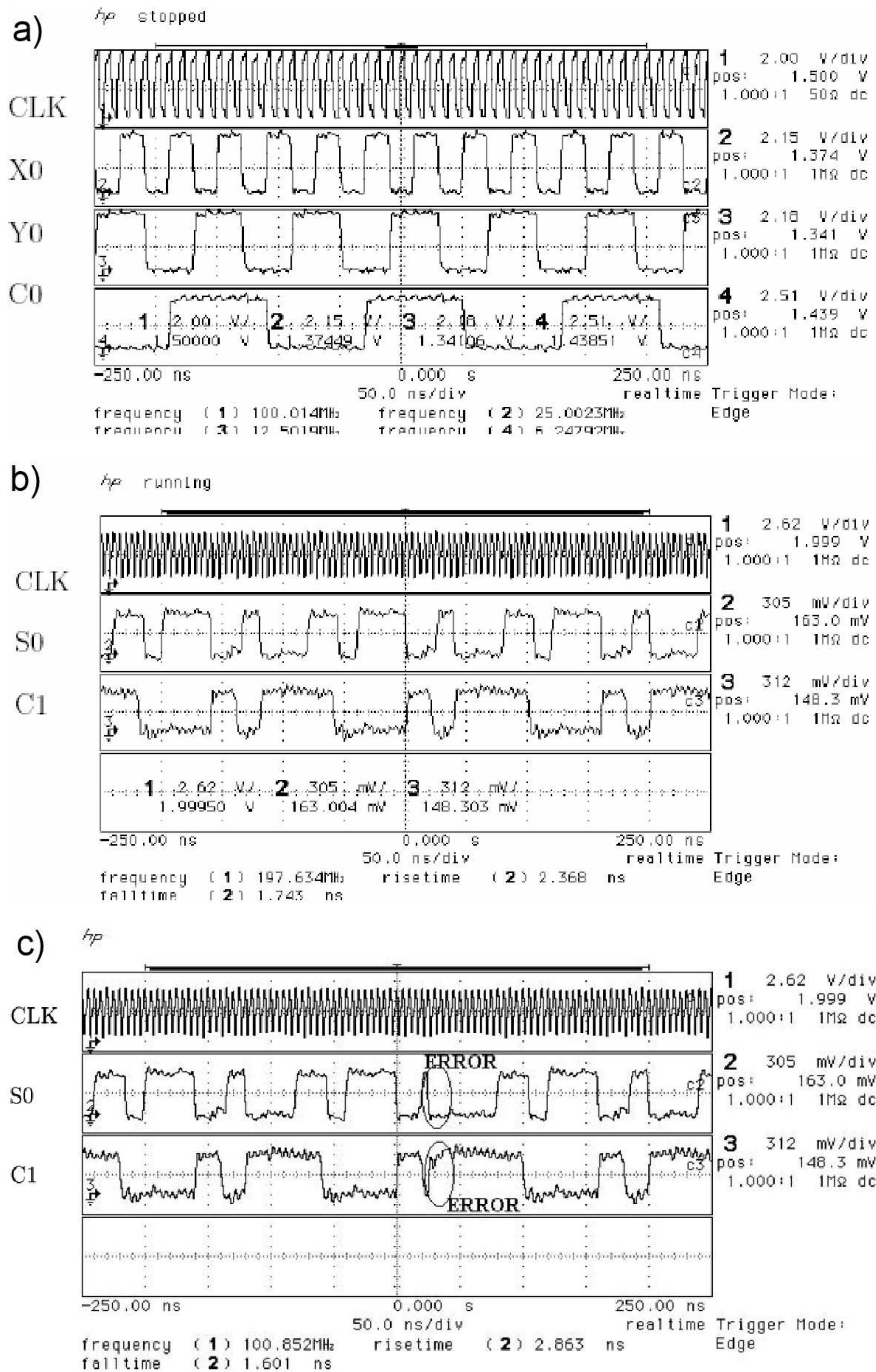


FIGURE 12. (a) Binary counter pattern input signals for the noise tolerant full adder with the NIC activated. (b) Correct pulse pattern at the outputs of the test circuit, and (c) when a noise pulse is applied to the test circuit, a logic error appears at the outputs.

TABLE III. Logic levels at the inputs of the test circuit to measure noise immunity.

Data	Logic level
X	LOW
Y	HIGH
C	LOW

TABLE IV. Average Noise Threshold Energy (ANTE) from the fabricated noise-tolerant full adder and the conventional full adder.

Test circuit	ANTE (V^2-ns)
Convencional TSPC full adder	1.63 (simulated)
Noise immune full adder	4.82 (measured)

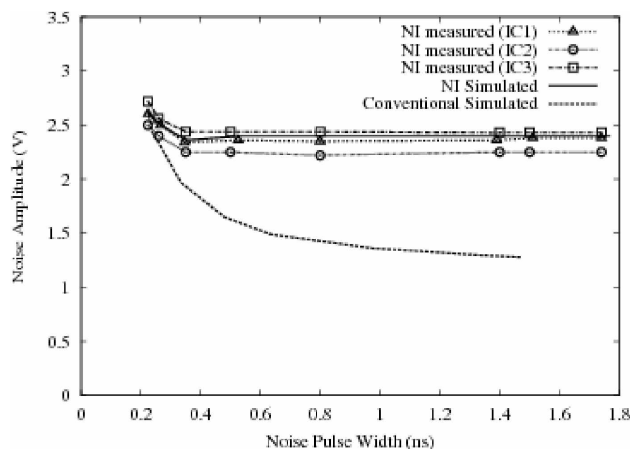


FIGURE 13. Experimentally measured noise immunity curve for the noise-tolerant adder and simulated noise immunity curve for the conventional adder.

6.2. Operation of the test circuit under noise injection

In this section, the operation of the noise tolerant full adder under injected noise pulses is shown. If a noise pulse with enough amplitude and width is applied to the victim node of the test circuit (node "a" in Fig. 9a), a logic error can appear at the output (s_0). Figure 12a shows the pulse pattern applied to the inputs to verify noise effects. When the noise pulse does not have enough amplitude and width, no logic failure occurs at the outputs (see Fig. 12b). On the other hand, if the noise pulse has enough amplitude and width to provoke an undesirable logic transition at the victim net, then the logic error is propagated through the outputs. Figure 12c shows this logic error.

6.3. Noise immunity curves of the noise-tolerant full-adder

To measure the noise immunity of the test circuit, the clock frequency is set at f_{CLK}=200 MHz and the inputs are adjusted at a fixed logic level as indicated in Table III. With these logic levels the victim node "a" is at "0" logic level; the resulting sum S_0 is "1" and the carry out C_1 is "0". The NIC is triggered with the clock signal in order to have a noise pulse every time the clock is HIGH (the evaluation phase for N-blocks). The voltage V_{NW} and the voltage V_{NA} in the NIC are adjusted to change the width and amplitude of the noise pulse until a logic failure is obtained at the outputs of the full adder, in other words until S_0 changes from "1" to "0" and/or C_1 changes from "0" to "1". The corresponding noise pulse width and amplitude are added in a width-amplitude graph to build the noise immunity curve. This process is repeated until the noise immunity curve is completed.

Figure 13 shows three experimentally measured noise immunity curves for three different fabricated chips. These curves are compared with the simulated (typical process parameters) noise immunity curve of the noise-tolerant adder as well as the noise immunity curve of the conventional adder. The increment in noise immunity for the full adder implemented with the proposed technique is evident from Fig. 13. Note that the simulated and experimental noise immunity curves of the noise-immune full adder agree quite well. Furthermore, these curves become almost constant from a pulse width of W_n=0.4 ns. This is because the transparency window was designed to have a width of 370 ps. After this time any noise pulse fails to have any effect on the output of the gate.

The average ANTE metric is obtained from the three experimental noise immunity curves to compare the noise immunities of the full adder implemented with the proposed technique and the conventional one quantitatively (see Table IV). The noise-tolerant full adder improves the ANTE metric 2.95 times over the conventional TSPC full adder.

7. Conclusions

The feasibility of a new noise-tolerant dynamic circuit technique has been shown by means of electrical simulations and experimental results. This technique can be easily implemented in dynamic precharge-evaluate gates like TSPC. The advantages of this new noise tolerant dynamic circuit technique are: (1) high noise immunity, (2) flexibility to implement the proposed technique in a wide variety of dynamic logic styles, (3) the pull down network of the gates is not modified, (4) trade-off between noise immunity and delay can be balanced to meet a specific delay, (5) adequate for large fan-in gates. The proposed noise-tolerant technique uses two strategies to improve the noise tolerance of dynamic gates: first, raising the noise threshold of the gate by precharging an internal node in the PDN. Due to body effect, the noise threshold of the gate is increased. Second, by isolating the dynamic node from the inputs when the PDN has been evaluated. This technique has been successfully applied to TSPC AND gates and the operating conditions of the proposed technique have been stated. The proposed technique has been compared with the conventional dynamic logic as well as other noise-tolerant techniques. The proposed noise-tolerant technique is validated experimentally in a relatively

complex test circuit (1-bit carry look-ahead full adder). The resulting noise immunity curves show that the proposed technique improves the noise immunity threefold with respect to a conventional dynamic full adder.

Currently, the proposed noise-tolerance technique in this paper is being applied in the design of complex logic blocks based on a standard cell library with noise tolerance [16].

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