MBE-growth and characterization of $In_xGa_{1-x}As/GaAs$ (x=0.15) superlattice

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A qualified $In_{0.15}Ga_{0.85}As/GaAs$ superlattice was grown on an n-type GaAs(100) substrate by molecular beam epitaxy(MBE). Analysis of this structure was first carried out by X-Ray diffraction(XRD) and this structure's the interface thicknesses, roughness and x concentration determined at nanoscale. Secondly, the electrical characteristics of this sample such as the current-voltage-temperature (I-V-T), capacitance-voltage-temperature (C-V-T) and conductance-voltage temperature (G-V-T) were studied over a wide temperature range. The energy distribution of interface states was determined from the forward bias I-V characteristics by taking into account the bias dependence of the effective barrier height. Experimental results show that the forward and reverse I-V characteristics are similar to Schottky-junction behavior. The ideality factor n, series resistance R_s, barrier height Φ_B and density of interface states N_{ss} were found to be strong functions of temperature. According to thermionic emission (TE) theory, the zero-bias barrier height (ϕ_{Bo}) calculated from forward bias I-V characteristics was found to increases with increasing temperature. In addition, the value of R_s as a function of both voltage and temperature was obtained from C-V and G-V characteristics. The temperature dependent of I-V, C-V and G-V characteristics confirmed that the distribution the R_s and N_{ss} are important parameters that influence the electrical characteristics of these devices.

Keywords: MBE; X-Ray diffraction; series resistance; interface states; temperature dependent.

Un cualificado $In_{0.15}Ga_{0.85}As/GaAs$ superenrejado ha sido desarrollado en un substrato de tipo n mediante una epitaxia de viga molecular (MBE). El análisis de esta estructura fue llevado a cabo, en primer lugar por una difracción de rayos X (XRD) y en esta estructura el grosor, la aspereza y la concentración x fueron determinadas del interfaz fueron determinados en una nano-escala. En segundo lugar, las características eléctricas de este ejemplo, tales como la actual temperatura del voltaje (I-V-T), la temperatura del voltaje capacitado (G-V-T) y la temperatura de la conductividad del voltaje (G-V-T) estudiados dentro de un amplio rango de temperaturas. La distribución energética de los estados del interfaz fue determinada de las características I-V del sesgo avanzado, teniendo en cuenta la dependencia diagonal de la altura eficaz de la barrera. Los resultados experimentales muestran como las características avanzadas e inversas I-V son similares al comportamiento de la juntura de Schottky. El factor ideal n, las resistencias en serie Rs, la altura de la barrera y la densidad de los estados del interfaz Nss resultaron ser funciones importantes de la temperatura. Según la teoría de la emisión termoiónica (TE), la altura de la barrera del sesgo cero, calculada de las características del sesgo avanzado I-V resultaron aumentar con un aumento de la temperatura. Al mismo tiempo, el valor de R y la juntura del voltaje y la temperatura se obtuvieron de las características C-V y G-V. La temperatura dependiente de las características I-V, C-V y G-V confirmaron que la distribución de las R y N son parámetros importantes que influyen en las características eléctricas de estos mecanismos.

Descriptores: MBE; difracción de rayos X; serie de la resistencia; interfaz fueron; temperatura dependiente.

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1. Introduction

The lattice mismatched $In_{0.15}Ga_{0.85}$ As / GaAs structures have been the subject of extensive study in recent decades, because of their potential for integration of high speed GaAs electronics with opto-electronic devices [1]. Schottky diodes, field effect transistors(FET) and photo-detectors are prepared from GaAs and InGaAs based nanodimensional strained heterostructures. Currently in the production of nanodimensional multi quantum wells and quantum dots, molecular beam epitaxy (MBE) is used rather than other growth techniques [2, 3].The reflection high energy electron diffraction (RHEED) technique has been widely applied to the study of MBE growth kinetics. RHEED oscillations at the onset of growth have been used both to measure growth rates, and to accurately determine alloy compositions and surface diffusion lengths [4].

In the present work, structural and electrical characteristics of $In_{0.15}Ga_{0.85}As$ /GaAs grown by MBE have been investigated. The interface thicknesses, roughness and x concentration at the nanoscale were verified by high resolution X- Ray diffraction (HRXRD). InGaAs/GaAs structure has a series resistance R_s, which causes the voltage drop across the junction to be less than the voltage applied between the terminals of the structure. Especially, forward bias current-voltage $(I-V)$ and admittance ($C-V$ and $G-V$) characteristics at high voltages deviate considerably from ideal behavior due to the effect of parameters such as R_s and N_{ss} [5]. We investigated the effects of the N_{ss} and R_s behavior on the electrical characteristics of $In_{0.15}Ga_{0.85}As/GaAs$ superlattices, and we carried out a systematic investigation on the voltage and temperature dependence of the electrical properties of these structures.

2. Experimental details

$In_{0.15}Ga_{0.85}As$/GaAs superlattices were fabricated on 3-inch diameter epi-ready GaAs (100)[Si doped ($n_{si} \sim 10^{18}$ cm^{-3})] substrate in a V80H-MBE system using elemental sources for Ga, In and As beams. The $In_{0.15}Ga_{0.85}As$/GaAs superlattice grown for the present study is shown schematically in Fig. 1. The superlattice was intentionally undoped but it shows n-type behavior since it has the background net doping concentration with donors [6]. The growth rate and reconstruction of the (100) surface were determined by RHEED oscillations. A transition of the amorphous circular pattern to a 2×4 streaked pattern and the surface oxide desorption has been observed as the substrate is heated above 580°C. After that the substrate temperature was lowered to 560°C for the growth of the entire epitaxial structure. During growth, beam equivalent pressures (BEP) for As_2 and Ga are kept at 1.3×10^{-5} mbar and 7.9×10^{-7} mbar, respectively. Growth rates of GaAs and InAs were 2.780 Å/s and 3.058 Å/s, respectively. For the structure, 500 nm GaAs buffer layer growth followed by deposition of five period a 5nm/25nm InGaAs/GaAs layers as shown in Fig. 1.

The HRXRD measurements were performed by a D8-Discover diffractometer equipped on the primary side with a Ge (220) monochromator and a horizontal divergence slit with a width of 1mm. On the secondary side, the reflected light passes through a horizontal slit of 0.1 mm wide before entering the wide open scintillation detector.

High purity Au with a thickness of $\sim$ 2000 Åwas thermally evaporated onto the whole back side of the wafer. The ohmic contact was formed by sintering the evaporated Au back contact at 400°C in a high vacuum. For the rectifier contact $\sim$ 2000 Åthick Au dots with an area of 0.011 cm^2 were evaporated onto the front surface.

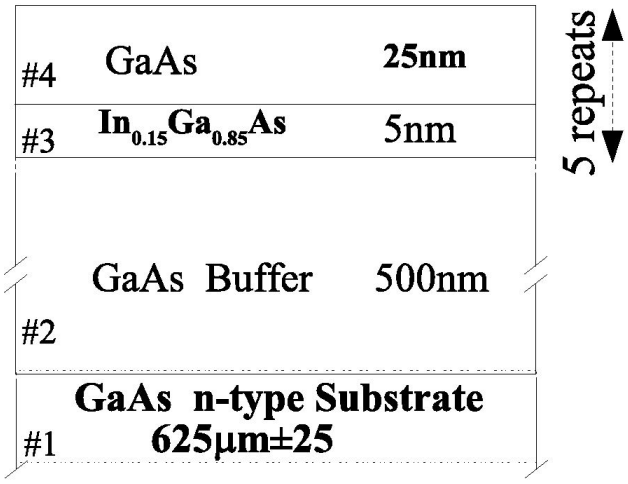

FIGURE 1. Schematic structure of $In_{0.15}Ga_{0.85}As$/GaAs

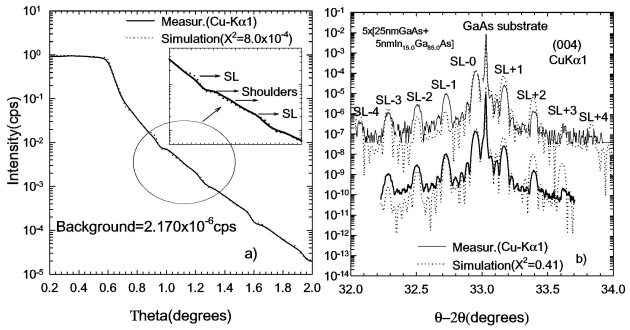

FIGURE 2. a) Intensity of XRR of 5× multi quantum well sample. b) High-resolution Bragg diffraction in the vicinity of the (004) reflection of 5× multi quantum well stack. Solid lines show experimental data and dotted lines give fit curves.

3. Result and discussion

3.1. X-Ray Diffraction Measurements

X-ray reflectivity (XRR) scan for the azimuthal orientation of the sample were performed using $CuK_{\alpha 1}$ radiation as shown in Fig. 2a. In principle, the thicknesses of the layers, their chemical compositions as well as the root mean square roughnesses (rms) of the interfaces can be obtained from such measurements. As shown in Fig. 2a, the plateau region in the approximately $0 - 0.6^\circ$ interval is strongly smooth, which suggests that sample surface is uniform.

In Fig. 2a, the measured specular reflection curves exhibit weak periodical satellite maxima, their height is influenced by the interface roughness and by the thickness of the individual layers building up the multilayer period. Surprisingly, it depends on the direction of the incident X-ray beam. it is shown clearly in the inset figure of Fig. 2a that there is a more or less pronounced symmetric shoulder associated with each maximum, indicating highly symmetric interfaces. In addition, there is an strong contribution of a background which also depends on the sample orientation. After subtracting a diffuse background, a best fit is obtained with a thickness of 4.0174 nm($\pm$0.1%) for the (In,Ga)As layers with an rms roughness of σ =1.9889$\pm$ 0.1 nm and 20.289 nm($\pm$0.1%) for the GaAs layers with an rms roughness of σ = 1.3519$\pm$ 0.1 nm. For an X-ray incidence angle α less than some critical value (*i.e.*, $\alpha < \alpha_c$), the incident X-ray beam is totally reflected at the air-layer interface. Above the critical angle of incidence, the intensity of the scattered X-ray intensity falls by several orders of magnitude. The measurement of the critical angle of incidence α_c can be used to estimate of the density of the ternary layer. As shown in Table I, there is neither appreciable change in the density of the ternary layer nor any formation of GaAs layers, since the density values obtained from the simulation curve found by fitting to the experimental curve are in perfect agreement with the known theoretical densities. Reflectivity measurements were simulated by the LEPTOS program, which is supported by the simulated annealing method [7]. This is a global optimization method derived from Monte Carlo methods.

TABLE I. Simulation results obtained from XRR and HRXRD. The numbered # symbols show the layers given in Fig. 1

	Density		Thickness		Roughness	In
	Experimental	Theoretical				Content
	± 0.03 g/cm^2	g/cm^2	$\pm 1\%$ nm		± 0.1 nm	%
	XRR	-	XRR	HRXRD	XRR	HRXRD
#4	5.3176	5.3176	20.289	18.788	1.352	-
#3	0.9756	1.000	4.0174	4.8991	1.989	15.10

In Fig. 2b, we have plotted conventional high resolution five crystal rocking curves obtained with $CuK_{\alpha 1}$ radiation for the symmetrical (004) Bragg diffraction with k along the [110] direction. In this figure, the simulation of the HRXRD scan using the computer program [8] based on the solution to the Takagi-Taupin equations of dynamical diffraction theory is also given in Ref. 8. As shown in the figure, two different diffractions in the middle and near the edge of the wafer are taken. These curves give similar results, and the parameters calculated from each diffraction pattern are averaged.

For the accurate HRXRD measurements, the position of the sample was adjusted in order to provide maximum intensity from the substrate peak. Good agreement between experiment and simulation is obtained with a layer sequence of 5$\times$ (18.7878 nm GaAs, 4.8991 nm $In_{15.1}Ga_{84.9}As$, placed on a GaAs buffer) assuming a perfect tetragonally distorted layer system. Because, in strain analysis, dc_1/c bottom and dc_2/c top which are the normal (perpendicular to the sample surface) lattice mismatches are obtained from simulation as same values (2.619×10^{-7}). Here c is the lattice constant of the substrate and dc_1/dc_2 is the difference between the substrate's lattice constant and the layer's bottom/top lattice constant. These values clearly prove that at each period, the strain of $In_{0.15}Ga_{0.85}As$ layer perpendicular to surface, is conserved on a large scale during growth of this layer. It should be noted that the symmetrical (004) reflection is only sensitive to the lattice strain perpendicular to the layers. The values obtained from the HRXRD measurements are collected to compare with XRR in Table I. It shows that there is a good agreement between any two measurements.

The angular position of the 0^{th} order superlattice peak was determined by calculating the mean In content in the whole superlattice system in the growth direction, which is 15.1%. On the left hand side of the substrate peak, superlattice satellite peaks up to the order -4 are visible. On the right hand side, the superlattice peaks +1 to +4 can be observed and some of these peaks are weak as seen in Fig. 2b. The disappearance of the superlattice peak is due to destructive interference effects depending critically on the individual layer thicknesses.

3.2. The temperature dependence of the electrical characteristics

For a structure of Au/$In_{0.15}Ga_{0.85}As$/GaAs with a uniform thin oxide insulator layer, it is assumed that the relationship between the applied forward bias ($V > 3kT/q$) and the current of the structures is due to pure thermionic emission (TE) theory and it can be expressed as [9–11]

$$I = I_0 \exp\left[\frac{qV}{kT}\right]\left[1-\exp\left[\frac{-qV}{kT}\right]\right], \qquad (1)$$

where k is the Boltzmann constant, T is the temperature in Kelvin and V is the applied voltage. As a refinement of this method, the series resistance R_s due to the bulk and contact resistance and the so-called ideality factor n were introduced, to include the contributions of other current-transport mechanisms. Then:

$$I = I_0 \exp\left[\frac{q(V-IR_s)}{nkT}\right]\left[1-\exp\left[\frac{q(V-IR_s)}{kT}\right]\right], \qquad (2)$$

where I_o is the reverse saturation current and expressed as

$$I_0 = A^* A T^2 \exp\left[\frac{-q\Phi_{Bo}}{kT}\right], \qquad (3)$$

where the quantities A^*, A and Φ_{Bo} are the effective Richardson constant, the area rectifier contact and zero-bias barrier height, respectively.

The $ln(I) - V$ characteristic for one of the Au/$In_{0.15}Ga_{0.85}$ As/GaAs in the temperature range from $210 - 400$ K are shown in Fig. 3a. The zero-bias barrier height ϕ_{Bo} and diode ideality factor n values were calculated according to Ref. 9 as shown in Table II. The ϕ_{Bo} values calculated from $I - V$ characteristics show an unusual behavior that increases with the increase in temperature. This temperature dependence is in obvious disagreement with reported negative temperature coefficients of the barrier height. Due to interfacial oxide layer and density of interface states N_{ss} in equilibrium with the semiconductor, the ideality factor n becomes greater than unity, as proposed by Card and Rhoderick [11], and is given by

$$n(V) = 1 + \frac{\delta}{\varepsilon_i}\left[\frac{\varepsilon_s}{W_D} + qN_{ss}\right], \qquad (4)$$

TABLE II. Temperature dependent values of various parameters determined from I-V characteristics of Au/ $In_{0.15}Ga_{0.85}As$/n-GaAs.

T(K)	I_o(A)	n	Φ_{B0} (I-V)(eV)
210	2.81×10^{-5}	4.634	0.340
245	2.73×10^{-5}	4.101	0.395
260	1.88×10^{-4}	2.965	0.388
320	5.45×10^{-4}	3.004	0.459
340	6.42×10^{-4}	2.627	0.487
380	1.57×10^{-3}	3.420	0.522
400	3.23×10^{-3}	4.820	0.528

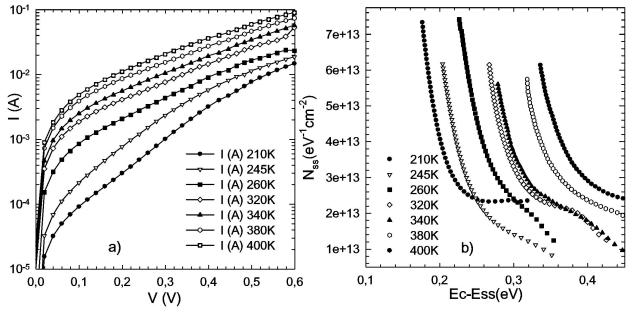

FIGURE 3. a) Forward bias $I-V$ characteristics of Au/$In_{0.15}Ga_{0.85}As$ / n-GaAs at different temperatures. b) Density of interface states N_{ss} as a function of E_c-E_{ss} deduced from the $I-V$ data at various temperatures.

where W_D is the space charge width, δ is the thickness of interfacial oxide layer, ε_s and ε_i are permittivities of the semiconductor and the interfacial oxide layer, respectively. The native insulator layer thickness was obtained from sufficiently high frequency (f≥1 kHz) *C-V* characteristics such as 25Å by using the equation for the insulator layer capacitance of $C_i=\epsilon_i\epsilon_o A/\delta$, where, ϵ_i and ϵ_o are the permittivity of the interfacial layer and free space, respectively.

We observed a deviation from the ideality in the electrical characteristics because of roughness, density of interface states and series resistance of the structure. The high value of the ideality factor was attributed to the inhomogeneity of the potential barrier height. Also, at low temperatures carriers with low energy may exceed the lower potential height.

In recent years lattice-mismatched III-V semiconductor heterostructures have found promising technological applications because of a high flexibility in tailoring their physical properties, especially the electrical and structural ones. The pseudomorphic epitaxial growth of such heterostructures is accompanied by elastic strain, arising at the interface, which affects the electronic structure of the layers, *i.e.* changes the band gap energy, reduces or removes the interband or intraband degeneracies or induces coupling between neighboring bands and the variety of values of the ideality factor [12]

According to [13–16], the ideality factor of an inhomogeneous Schottky Barrier Diodes (SBD) with a distribution of low Schottky Barrier Heights (SBHs) may increase with a decrease in temperature. Schmitsdorf *et al.* [16] used Tung's [13] theoretical approach and they found a linear correlation between the experimental zero bias SBHs (Φ_{Bo}) and the ideality factors. However, in this study, as can be seen from Table II, there is no linear relationship between the experimental Φ_{Bo} and n of the $In_xGa_{1-x}As$/GaAs (x=0.15) superlattice.

In the n-type semiconductors, the energy of the N_{ss} with respect to the bottom of the conductance band E_c, at the surface of the semiconductor, E_{ss} is given by [10]

$$E_c-E_{ss}=q(\phi_e-V), \tag{5}$$

where ϕ_e is assumed to be bias-dependent due to the presence of an interfacial layer and is given as

$$\phi_e=\phi_{Bo}+\left[1-\frac{1}{n\,(V)}\right](V-IR_S)\,. \tag{6}$$

For each temperature, the energy distribution of N_{ss} can be thus obtained from experimental data for this region of the forward bias I-V in Fig. 3a. Figure 3b shows the resulting dependence of the N_{ss} profile converted to a function of E_{ss} at various temperatures.

We have found that the mean values of N_{ss} decreases with increasing temperatures. This behavior is attributed to the molecular restructuring and reordering of insulator-semiconductor interface under the temperature effect [12]. From Fig. 3b, it can be seen that an exponential increase in the N_{ss} exists from midgap towards the bottom of the conduction band [5, 17].

The $C-V$ and $G-V$ measurements were carried out for the $In_{0.15}Ga_{0.85}$ As / GaAs structure at various temperatures at 5 MHz. As shown in Fig. 4a , the $C^{-2}-V$ plots for each temperature are linear over the voltage range -0.8V≤V≤-0.2V. This linear behavior of $C^{-2}-V$ plots shows that the measurements are made at a sufficiently high angular frequency ($w=2\pi f$) and the change in density of the interface states cannot follow the a.c. signal [18,19]. The $C^{-2}-V$ characteristics of a minority carrier can be described by [20]

$$C^{-2}=(2/q\varepsilon_s A^2 N_D)\,(V_0+V_R)\,, \tag{7}$$

where V_0 is the built-in voltage, q is the electronic charge, V_R is the reverse bias voltage and N_D is the doping concentration. The barrier height is obtained from Fig. 4a and it is given by [21]

$$\phi_B\,(C-V)=V_D+E_F-\Delta\phi_B, \tag{8}$$

where $\Delta\phi_B$ is the image force barrier lowering and its very low values in the calculation of barrier height $\phi_B(C-V)$ can be neglected. E_F is the Fermi energy level and V_D is the diffusion potential, which are given by

$$E_F=\left(\frac{kT}{q}\right)\ln\left(\frac{N_c}{N_D}\right), \tag{9}$$

$$V_D=V_{_0}+\frac{kT}{q}, \tag{10}$$

TABLE I. Temperature dependent values of various parameters determined from C-V characteristics of Au / $In_{0.15}Ga_{0.85}As$ / GaAs structure.

T(K)	$N_D(cm^{-3})$	E_F(eV)	W_D(cm)	Φ_B (C-V)(eV)
80	$4.42\times10^{+15}$	0.051	1.61×10^{-09}	1.21
120	$4.41\times10^{+15}$	0.076	1.60×10^{-09}	1.16
160	$8.83\times10^{+15}$	0.092	8.02×10^{-10}	2.10
220	$7.36\times10^{+15}$	0.130	9.62×10^{-10}	0.73
225	$5.52\times10^{+15}$	0.131	1.28×10^{-09}	0.55
240	$1.10\times10^{+16}$	0.134	6.41×10^{-10}	1.35
320	$8.83\times10^{+15}$	0.184	8.02×10^{-10}	1.61

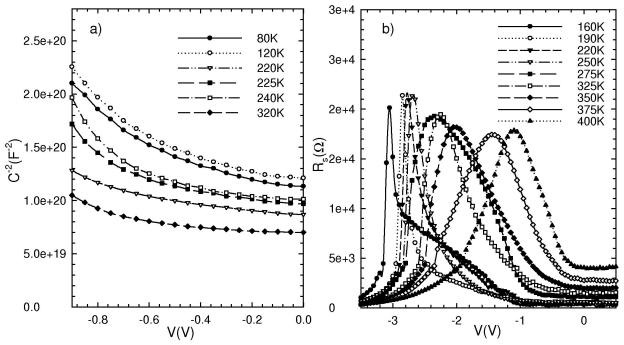

FIGURE 4. a) Plot of $1/C^2$ vs V of Au / $In_{0.15}Ga_{0.85}As$ / GaAs for different temperatures at a frequency of 5000 kHz. b) The $R_s - V$ plot of Au/$In_{0.15}Ga_{0.85}As$/n-GaAs structure for different temperatures at a frequency of 5000 kHz.

where V_o is the voltage intercept of the $C^{-2} - V$ plots, Nc is the effective density of states in the GaAs conductance band and N_D is the carrier doping density determined from the slope of the linear plot $C^{-2} - V$ curves. The temperature dependence of N_D, E_F, W_D and Φ_B values are obtained from $C^{-2} - V$ plot and are presented in Table III. Before any analysis, all the measurements must be corrected for series resistance. The values of R_s are calculated from the measured admittance when the structures are biased in strong accumulation [19]. In addition, voltage dependence of the R_s can be obtained from the measurements of $C - V$ and $G - V$ curves. According to Ref. 12, series resistance is given by

$$R_s = G_{ma}/(G_{ma}^2 + (\omega C_{ma})^2), \qquad (11)$$

where C_{ma} and G_{ma} represent the measured capacitance and conductance values, respectively, in the strong accumulation region.

$R_s - V - T$, as a parameter, are shown for a signal frequency of 5000 kHz in Fig. 4b. While the values of series resistance decrease with increasing temperature in accumulation region, they increase with increasing temperature in depletion and reverse regions. Such behavior of the series resistance R_s has been attributed to atomic distribution and reconstruction of density of interface states distribution profiles N_{ss} [9].

4. Brief summary

In summary, an $In_{0.15}Ga_{0.85}As$/GaAs superlattice has been grown on an n-type GaAs(100)-($2t\times4$) surface at a substrate temperature 560°C by MBE. Analysis of the X-ray diffraction results allows for a direct determination of the composition and periodicity of each superlattice structure grown. The measured composition and layer thicknesses are found to be approximately equal to the desired (nominal) values. Experimental results show that the zero-bias barrier height ϕ_{Bo} increases with an increasing temperature while series resistance R_s and density of interface states N_{ss} decrease. The series resistance profile of these structures versus applied voltage at each temperature gives a peak and the peak positions shifted to a negative bias. This behavior may be a result of molecular restructuring and reordering of the metal semiconductor interface.

Acknowledgements

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