An on-chip magnetic probe based on MOSFET technology

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An original application for a magnetic field-sensitive Split-Drain MOSFET (MAGFET) used to monitor both the integrity of the electrical signal on-chip, as well as the magnetic flux density radiation on-chip is presented in this work. We introduce experimental and simulation results of a test chip that prove static and low-frequency on-chip generated magnetic fields that can be detected on-chip leading to a fluctuation in the drain current (ΔI_{DS}) of a MAGFET device. The design of this first version of the test chip is intended for DC characterization as the pads, package and wiring do not allow going above a frequency of 300 MHz. In this particular case of a 0.5 μm CMOS technology and the used dimensions, the cutoff frequency of the test MAGFET is in the range of 500 MHz to 1 GHz depending on the bias conditions. For the static and low-frequency case used in this experimental work the capacitive coupling between the interconnect line and the gate electrode is negligible. The current in the interconnected line, that varies from 500 μA to 35 mA, generates a magnetic flux density at a rate of 100 μT/mA. When these magnetic lines cross through the channel of the MOS transistor, an electromagnetic coupling rate (ΔI_{DS}/B) as far as 1.5 μA/mT is induced. We observed that from the 0.7, 0.5, and 0.35 μm characterized MOS technologies data, the (ΔI_{DS}/B) rate increases with the miniaturization process of fabrication technology. This electromagnetic rate reduces as the temperature is increased from 20 to 120°C. From numerical simulations we conclude that this phenomenon is attributed to the way carrier mobility and inversion channel charge interplay with the on-chip tangential and perpendicular components of the (B) field. Having an array of MAGFETs distributed on the surface of the chip would serve to monitor the EM radiation, which in turn may be used for estimation and mitigation of RF interference. These results allow establishing the basis for a future development for on-chip magnetic probe for nanometer MOS technologies.

Keywords: Magnetic field measurement; integrated sensor; magnetic field-effect transistor (MAGFET); hall effect; radiation on-chip.

En este trabajo se presenta la pertinencia de utilizar transistores de efecto de campo sensible a campo magnético con drenaje múltiple (Split-Drain MAGFET) en el monitoreo tanto de la integridad de la señal eléctrica así como de la radiación de la densidad de flujo magnético, ambos a un nivel on-chip. A lo largo de este artículo se muestran resultados experimentales y simulados de un circuito integrado de prueba en donde se resalta la capacidad del dispositivo MAGFET en detectar campos magnéticos estáticos o dependientes del tiempo a baja frecuencia, generados a nivel on-chip, a través de un desbalance en la magnitud de las corrientes de drenaje (ΔI_{DS}). El diseño de esta primera versión está enfocado hacia la caracterización en corriente continua debido a que los contactos, empaquetado y alambrado limitan la frecuencia de operación por debajo de los 300 MHz. En este caso particular, tecnología CMOS-0.5 μm, la frecuencia de corte del MAGFET se encuentra en el rango de los 500 MHz a 1 GHz dependiendo de las condiciones de polarización. En aplicaciones de campo magnético estático o de baja frecuencia llevados a cabo en este trabajo experimental, el acoplamiento capacitivo entre la línea de interconexión y el electrodo de compuerta es despreciable. La corriente en la línea de interconexión, variando de 500 μA a 35 mA, genera una densidad de flujo magnético a una razón de 100 μT/mA. Cuando estas líneas magnéticas cruzan el canal del transistor, una razón de acoplamiento electromagnético (ΔI_{DS}/B) de 1.5 μA/mT es posible de alcanzar. Se observa que a partir de datos experimentales provenientes de tecnología MOS de 0.7, 0.5 y 0.35 μm, es posible proyectar una relación inversamente proporcional con (ΔI_{DS}/B), esto es, la razón de acoplamiento electromagnético se incrementa con respecto al escalamiento de dimensión de la tecnología. Sin embargo, esta razón de acoplamiento se ve reducida conforme se incrementa la temperatura de operación de 20 a 120°C. A partir de simulaciones numéricas, se concluye que este fenómeno es atribuido a la manera en que la movilidad de los portadores de carga y la carga de inversión en el canal interactúan con la componente tangencial y perpendicular del campo (B) generado a nivel on-chip. El contar con un arreglo de dispositivos MAGFET distribuidos sobre la superficie del chip haría posible, a través del monitoreo de la radiación electromagnética (EM), estimar la interferencia por radiofrecuencia. Estos resultados permiten establecer las bases para un desarrollo futuro de probadores magnéticos integrados para tecnologías MOS nanométricas.

Descriptores: Mediciones de campo magnético; sensor integrado; transistor de campo magnético (MAGFET); efecto hall; radiación en chip.

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1. Introduction

Initial awareness of potential electromagnetic compatibility (EMC) problems is a crucial factor in the design process of modern electronic systems. Although integrated circuits (IC) are generally the ultimate source and/or victim of an EMC problem, the focus of most EMC-related research and problem solving has been external to the IC package [1]. As

the operating frequencies, as well as the number of transistors being integrated on a single die, increase, also the radiated and conducted electromagnetic emissions of ICs do. ***In fact, as well as the integration density increases and because of faster operating frequencies are present, large current flows during a short period of time through the power supply interconnections that are integrated on silicon, the IC package frame and the bonding wires leading to radiation of electromagnetic fields.*** For these reasons, in recent years IC electromagnetic emissions (EME) have become one of the selection criteria and for this purpose several measurements techniques have been proposed and some of them have been selected by regulatory committees as standard methods [2]. Depending on the frequency and the physical settings of the system, either a printed circuit board (PCB) or an integrated circuit, the interference or coupling may occur through one of the two modes. Since the energy in the reactive near-field is contained in the near magnetic field, a high precision magnetic probe is highly desired for the EMI measurement. In previous work [5], a thin-film magnetic field probe with a high spatial resolution was developed in order to obtain the absolute value of high-frequency power current on a large scale integration (LSI) chip. On another front, electro-optic (EO) and magneto-optic (MO) probes have received attention as minimally-invasive probes [6]. However, all these passive testing elements have a fundamental tradeoff between their sensitivity and spatial resolution. Additionally, they have also an incompatibility between spatial resolution and test efficiency because mechanical scanning with a small-sized single probe requires too much time for the measurement of the system. To solve these problems, we have proposed an on-chip magnetic probe based on a magnetic field-sensitive Split-Drain MOSFET (MAGFET) device as an active element. Many integrated magnetic sensor circuits use a MAGFET structure as a sensing element [7-9]. The MAGFET is a MOSFET with a single gate and two or more symmetrical drains sharing the total channel current. An imbalance between drain currents occurs because of the influence of a perpendicular magnetic field (B_Z) with respect to the gate plane. In spite of its large offset, temperature drift and noise, the MAGFET remains a popular magnetic field sensing device because of its easy integration with other electronic signal conditioning blocks in silicon chips. The flow of current in VLSI devices induces on-chip electromagnetic (EM) signals, as demonstrated by Slattery [10].

In this work we introduce experimental evidence that proves that the magnetic flux density component B couples back into the chip inducing a ΔI_{DS} fluctuation. Depending on the magnitude of the current of the on-chip interconnect line (I_{LINE}); the on-chip magnetic flux density magnitude varies from a few μT up to tens of mT [11]. The interaction of B with I_{DS} induces the current fluctuation or imbalance $\Delta I_{DS} = I_{DS1} - I_{DS2}$. The perpendicular component of the magnetic flux density induces a horizontal deflection of the channel current lines, whereas the tangential one B_Y induces a vertical deflection. The third component B_X, which is parallel to the channel, does not induce any deflection. The EM coupling rate (ΔI_{DS}/B) for the 0.7, 0.5, and 0.35 μm MOS technologies are measured at different bias level and temperature conditions. The experimental results are compared to EM Minimos-NT numerical simulations [12], which serves to conclude that the magnitude of interference or EM coupling is attributed to the fluctuation of both the inversion channel charge and electron mobility. The numerical simulation predicts the EM coupling is stronger for deep submicron MOS technologies with thinner gate oxides. In the following sections, the working principle of the Split-Drain MAGFET is described, including some theoretical aspects of the device behavior. Details on the real prototype are given along with the experimental assessments of the working principle and characterization of the device under test (DUT). In particular, a static magnetic flux density characterization of the device is provided, and some preliminary considerations on the time-varying magnetic flux density behavior of the MAGFET are also included.

In order to get physical insight into the MAGFET sensor, a brief review is presented in Sec. 2. In Sec. 3 the variation of the gate oxide thickness influence on the (ΔI_{DS}/B) ratio is presented through simulations validated with Minimos-NT. Experimental results of the nMOS MAGFET fabricated in a 0.5 μm CMOS technology used to monitor both the integrity of the electrical signal on-chip under steady-state as well as transient magnetic flux density are discussed in Sec. 4. Finally, some conclusions are summarized in Sec. 5.

2. Brief review of MAGFET device

The high sensitivity and CMOS compatibility of magnetic field-sensitive Split-Drain MOSFETs (MAGFETs) make this type of sensor a well-suited device for the integration of micromachined sensors and sensor signal processing, in addition this allows cost-effective batch fabrication and integration of on-chip biasing and readout circuitry [13-14]. Commercially available magnetic angle measurement systems are based either on magnetoresistive sensors or on two orthogonal mounted Hall sensors, whereas the sensing element in the present paper exploits galvanomagnetic effects in silicon using one single device. This approach permits superior performance. First, the sensing element has a smaller sensitive area, allowing magnetic flux density distribution to be considered as homogenous. Second, the galvanomagnetic effect in silicon is linear, allowing unrestricted angle measurements over the full 360° range.

The operation of the MAGFET is based on the Hall Effect principle. Inexpensive Hall effect sensors are generally made of silicon. The silicon devices have a sensitivity range of 10 to 1000 G or 10^6 to 10^8 nT [15]. Hall effect sensors can measure either a constant or a varying field; the upper frequency limit is about 1 MHz. Their power requirement is between 0.1 and 0.2 W, and they can be operated over an extremely wide temperature range limited only by packaging and lead attachment to the semiconductor. The physics law in a semi-

conductor is the formation of the Lorentz force (F_B)on an electrical charge (q) moving in a stable magnetic flux density with speed (υ)

$$F_B = q \cdot (\upsilon \times B_z) = q \cdot E_H \tag{1}$$

where E_H represents the equivalent Hall electrical field intensity. Because of the Lorentz force, the current equations in a semiconductor for electrons, in the presence of a magnetic field read as follows:

$$\vec{J}_n = \frac{1}{1+\left(\mu_n^* \vec{B}\right)^2}\Big[\left(q\mu_n n\vec{E} + qD_n\vec{\nabla}n\right) + \mu_n^*\vec{B}\times\left(q\mu_n n\vec{E} + qD_n\vec{\nabla}n\right)\Big] \tag{2}$$

here, B is the magnetic flux density, J_n denotes the electrons density, μ_n the drift mobility, μ_n^* the Hall mobility, n the electron concentration, D_n the diffusion coefficient, and E the electric field.

The device works electrically like a standard MOS transistor. The magnetic flux density measuring capability originates in the split drain. If a magnetic flux density is applied perpendicular to the device, the Lorentz force will deflect the charge carrier to one side. Thus the current in the corresponding drain will increase whereas the current in the other one will decrease, leading to a current difference. A circuital illustration of a MAGFET, including an interconnect line on the MAGFET's sensitive region, is shown in Fig. 1 for the sake of convenience.

The MAGFET structure is more attractive for applications such as non-contact switching, current measurement and magnetic memory readout because integrating it on chip with complex signal-processing circuitry requires nomodification of standard MOS fabrication process. The figure of merit for magnetic flux density resolution is B_{min}, the minimum detectable magnetic flux density. If the alpha $1/f$ noise parameter (α_H) of the sensor is constant, then B_{min} can be shown to be inversely proportional to the normalized sensitivity of the sensor. In the Split-Drain MAGFETs, the normalized sensitivity is defined as $\Delta I_{DS}/(I_{DS1}+I_{DS2})/B$. Some efforts have been developed using numerical models such as: finite element, Garlekin's residual method, and finite difference scheme [16] that are accurate but unfortunately obscure to explain device operation. A semi-analytic model based on semiconductor physics and electromagnetic theory has been investigated extensively in the past [17].

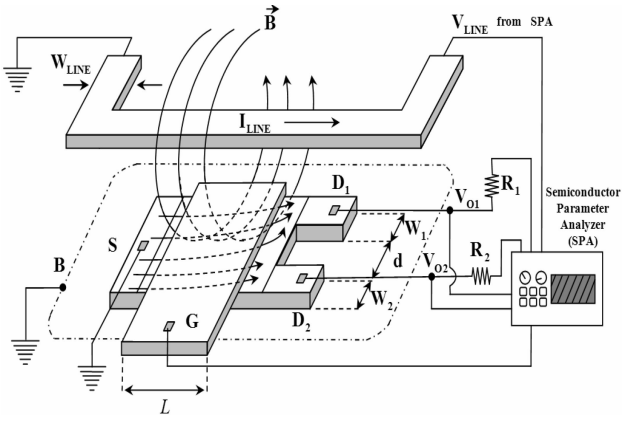

FIGURE 1. Illustration of a Split-Drain MAGFET with an on-chip interconnect line. W_{LINE} is the line width, $R_1$and R_2 are external resistor (994.2 Ω), I_{LINE}, ($V_{LINE}/R_{1,2}$) the current through the interconnect line, V_{LINE} the voltage applied to the line from the Semiconductor Parameter Analyzer, $\vec{B}$ the magnetic field, as well as B, S, D_1, D_2, G and d the substrate, source, drain 1, drain 2, gate terminals and drain distance of the MAGFET, respectively. L is the channel length; $W_1$and W_2 correspond to the width channel of both drains. Finally, V_{o1} and V_{o2} are the output voltage in each drain. The interconnect line is 6 μm away from the silicon surface.

3. Simulation results

The device being tested by this test circuit (MAGFET #3), used to characterize the magnetic flux density emission from aluminum interconnect lines and its EM interaction with the current I_{DS} of the MOS transistor, is a (W/L)=(70/70) nMOS transistor with drain distance of 20 μm, fabricated in a 0.5 μm AMIS CMOS technology [18]. The interconnect line, which is used as a magnetic flux density source, runs on top of the transistor (see inset in Fig. 2). The gate oxide thickness (T_{OX}) is 10 nm, and the interconnect line is a third level metal layer 6 μm away from the Si-SiO_2 interface. The width and thickness of the interconnect line, are 70 and 1.2 μm, respectively. 3D numerical simulations show 90% of the magnetic lines cross parallel to the Si-SiO_2 interface and perpendicular to the channel current. A second structure (MAGFET #1) [12], where six interconnect lines (three in the first and

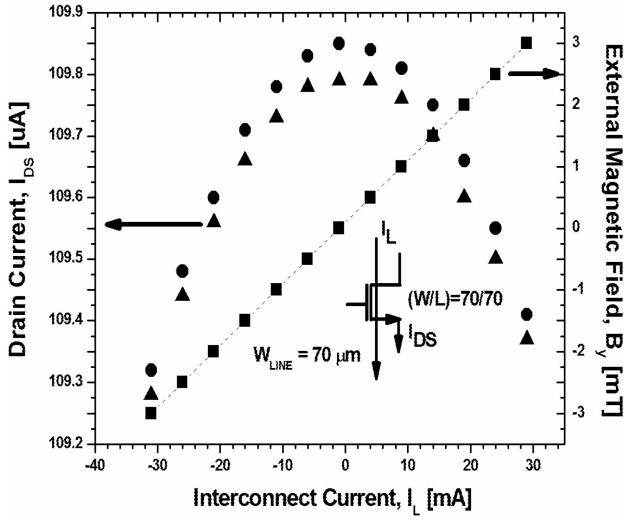

FIGURE 2. Measured I_{DS} current of one drain as a function of interconnect current I_{LINE}, and as a function of an external magnetic field B_Y (filled circle). The external B_Y is represented by the filled square in the right axis. V_{GS} = 1.0 V, V_{DS} = 0.1 V, T = 20°C. Inset shows the schematic representation of MOSFET and interconnects arrangement. Filled up-triangle represents simulation results.

three in the second metal layer) cross perpendicular to the channel axis, generates the perpendicular component of the magnetic flux density. The third device (MAGFET #2) is similar to MAGFET #3 but with (W/L) = (50/50), a drain distance of 10 μm and the interconnect line is a third level metal layer. Figure 2 shows the measured I_{DS} current versus the current I_{LINE} for MAGFET # 3. From positive to negative values of I_{LINE}, the resulting Lorentz force pushes electrons towards the Si-SiO_2 interface. A monotonic increase of I_{DS} should be expected when the inversion layer charge is pressed into the interface. However, this is only valid for I_{LINE} values down to +2 mA. To do a further exploration on this, an external magnetic flux density B_Y (filled square) applied parallel to the surface and perpendicular to I_{DS} produced the same fluctuation in ΔI_{DS} (filled circle in Fig. 2).

This demonstrated that ΔI_{DS} is correlated to the on-chip generated B_Y. By fitting both, the ($I_{DS} - I_{LINE}$) and ($I_{DS} - B_Y$) curves, the on-chip magnetic flux density generated by the interconnect line is extracted. The simulation results (filled up-triangle) reproduce the experiments very well. A further exploration on the simulations show the $I_{DS}-B_Y$ parabolic behavior is given by the spatial redistribution of the inversion charge as a function of B_Y and by the effect of surface scattering on the carrier mobility (see Fig. 3).

The I_{LINE} sweep from +35 mA to -35 mA induces an on-chip magnetic flux density B_Y from about +3 mT to -3 mT. This change of B from positive to negative values pushes electrons into the interface, increasing the effective inversion channel charge density (n_s), and increasing surface carrier mobility (μ_s) as well (see Fig. 3). However, as B_Y gets more negative, surface carrier scattering increases, which reduces mobility, and thus leads to a reduction of I_{DS}. The product of n_s and μ is what results in the parabolic-like behavior of the I_{DS}- I_{LINE} (or B_Y) curve. Once proved the interconnect line generates a B_Y field, we proceed to characterize the 0.7 and 0.35 μm MOS technologies by applying a B_Y equal to -3 mT. The measured ΔI_{DS} fluctuation, for the three different MOS technologies, as a function of its corresponding gate oxide thickness T_{OX} is shown in Fig. 4.

The magnitude of the magnetic flux density B_{max} at which the maximum value of I_{DS} is obtained, is not only given by the slope of n_s versus B_Y, but by the mobility μ as well. The experiment shows an increase of ΔI_{DS} at a rate proportional to ($1/T_{OX}$). The measured EM coupling rate ($\Delta I_{DS}/B_Y$) = is 0.15, 0.26, and 0.53 μA/mT for the 0.7, 0.5, and 0.35 μm MOS technologies, respectively. Additional experiments show the rate ($\Delta I_{DS}/B_Y$) reduces linearly with the increase of V_{GS} and increases with V_{DS} following the typical I_{DS}- V_{DS} relationship.

The perpendicular component B_Z induces a horizontal deflection of I_{DS}, which results also in a reduction of the I_{DS} current. In this case we use the second sample structure with an interconnect line crossing perpendicular to the channel axis of the MOS transistor, that results in a perpendicular cross of I_{DS} and B_X. By using the same measurement methodology as before, we obtained a ($\Delta I_{DS}/B_Z$) rate of 1.4, 1.5, and 1.55 μA/mT for the 0.7, 0.5, and 0.35 μm technologies, respectively. In the 20 - 120°C temperature range the measured (ΔI_{DS}/B) EM coupling rate reduces 1.4 nA/°C and 1.1 nA/°C for the B_Z and B_Y components, respectively (see inset in Fig. 3). This reduction is attributed to the reduction of mobility with the increase in temperature. The lower value of the temperature coefficient for the tangential component is attributed to the temperature dependence of the ($n_s\mu$) product.

4. Experimental results

In this section, we present the chip layout description and experimental characterization of the Split-Drain MAGFET

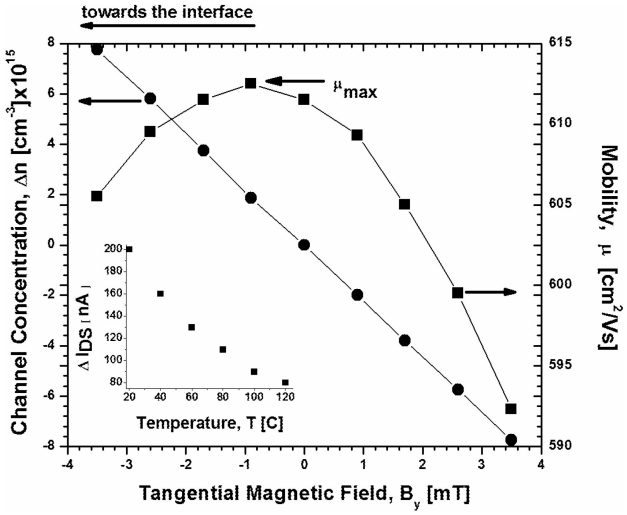

FIGURE 3. Simulated surface concentration fluctuation Δn_s (filled circle) and electron mobility μ (filled square) as a function of B_Y for the device under test. Δn_s= (n_s- n_s @ B_Y = 0 mT). Inset shows the temperature dependence.

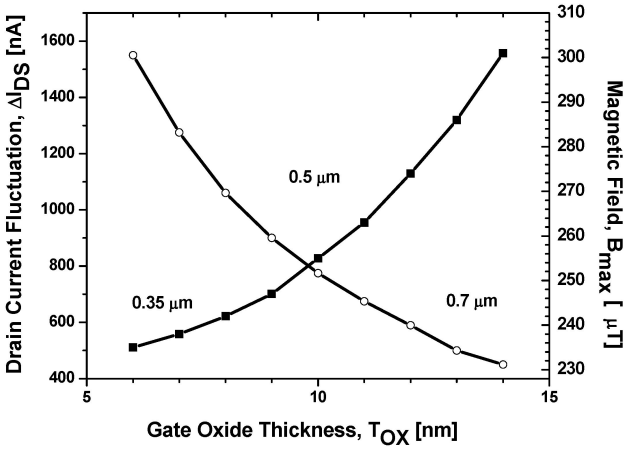

FIGURE 4. Measured drain current fluctuation ΔI_{DS} (filled square) and magnetic flux density (B_{max}) (hollow circle) corresponding to μ_{max} in Fig. 3, for different gate oxide thicknesses. Continuous line corresponds to simulations.

TABLE I. MAGFET specification.

Structure	(W/L) (μm)	Drain Distance (μm)	Type
# 1	(70/70)	20	NMOS
# 2	(50/50)	10	NMOS
# 3	(70/70)	20	NMOS

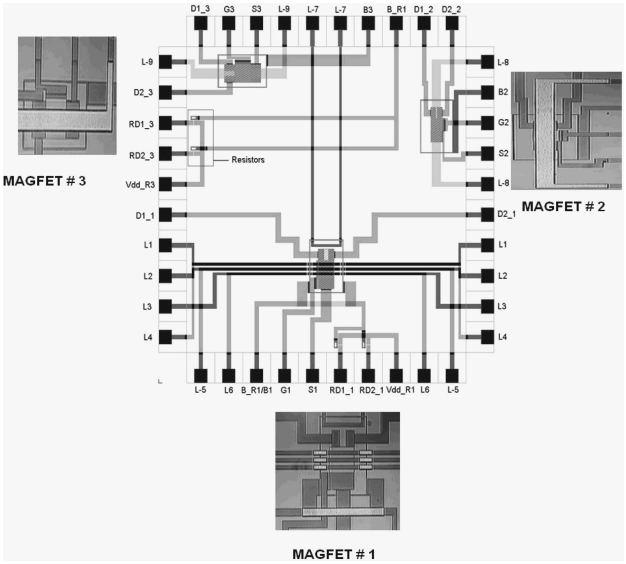

FIGURE 5. Picture showing floor plan and die configuration of two-drain MAGFET #1 (W/L) = (70/70), drain distance = 20 μm, MAGFET #2 (W/L) = (70/70), drain distance = 20 μm, and MAGFET #3 (W/L) = (50/50), drain distance = 10 μm. Included in the photograph are the metal level 1 and 2 integrated interconnect lines (perpendicular to the drain current) as well as metal level 3 (parallel to the drain current).

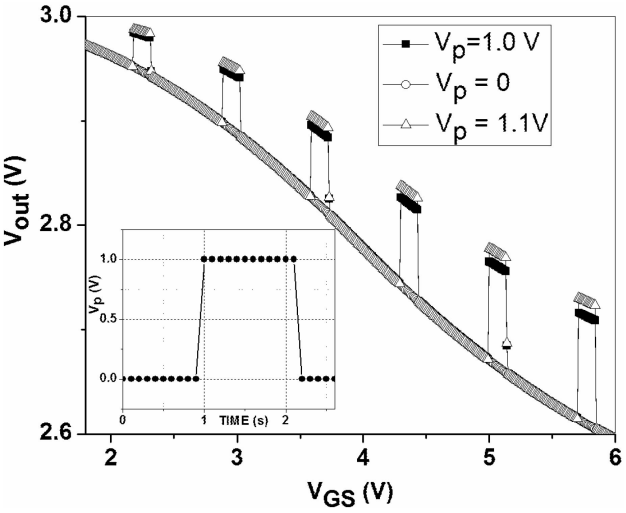

FIGURE 6. Measurement results of differential voltage (V_{OUT}) of MAGFET # 3 sensed by means of integrated resistors (R_{DD} = 994.2 Ω), *i.e.*, $V_{out} = I_{DS1}R_1 - I_{DS2}R_2$, connected to each drain. Inset shows the pulse voltage (V_P) generated by the SPA (voltage instead of current) and applied at the on-chip line #9 with 10 ns rise/fall times and T = 2 s (x axis is not at scale), $V_{DS1} = V_{DS2}$ = 200 mV.

structure proposed to monitor the magnetic flux density radiation. In Fig. 5, a photograph of the three MAGFETs devices as well as the chip floor plan are shown.

Specification of every single device is given in Table I. In this case, S3, G3, D1_3, D2_3 and B3, for instance, refer to as source, gate, drain 1, drain 2 and bulk pads for MAGFET # 3, respectively. Similar nomenclature was followed for the rest of the test structures. All experimental results showed in this work correspond to MAGFET # 3.

The chip design is made up of interconnect lines, where a current flows and generates a magnetic flux density, as well as three different MAGFETs structures. The width and separation of the interconnect lines were designed according to the current density specifications of the 0.5 μm AMIS CMOS technology. The dynamic response of the MAGFET is tied to the cutoff frequency of the CMOS used technology and its dimensions (width W and length L). In this particular case, the cutoff frequency of the test MAGFET is in the range of 500 MHz to 1 GHz depending on the bias conditions. For the static and low-frequency case used in these experimental work the capacitive coupling between the interconnect line and the gate electrode is negligible. However, we placed the interconnect lines as close as possible to the active region of the MAGFET with the aim to generate a magnetic field in the range of a few nano-Teslas.

The magnitude of the current determines the density of the magnetic lines. The MAGFET #1 consists of seven interconnect lines (Metal 1 and 2) layout above a two-drain MAGFET (perpendicular to the channel length), which then senses a differential current (I_{DS1}- I_{DS2}). One of these lines (#7) is outside the active region. The rest of the two-drain MAGFETs (# 2 and # 3) are made up of one metal stripe (metal 3) of 40 μm wide above each one and parallel to the channel length. In addition, four integrated resistors (R_{DD} = 946.4 Ω) were fabricated on poly-2 level and utilized in order to turn the drain current imbalance into a differential voltage drop. Considering the approximation of the interconnect line as an infinite segment of wire, the magnetic field intensity created was estimated through the well-known relation

$$B = \frac{\mu_o I_{LINE}}{2\pi s} \tag{3}$$

where μ_o is the permeability of free space, I_{LINE} the steady current and s the distance from the source to the evaluation point. All data measurements were taken using the *SPA Agilent 4155-C* and *Agilent 16442A Test Fixure*. All voltage or currents applied to the interconnection lines were generated through the *Agilent 41501B SMU and Pulse Generator Expander.*

Unfortunately, to the best of our knowledge, the present version of Minimos-NT is not able to perform an electrical device simulation for the case of time-varying magnetic flux density $B_Z(t)$. For this reason, only experimental results will be presented. In previous work of one of the authors [19], measurements data of MAGFETs devices with different (W/L) ratio, operated at linear region and under

conditions of room as well as nitrogen liquid temperature, showed the capacity to detect time-varying magnetic fields with frequency $\sim$ 10 Hz. At that time, an electromagnet was used to apply the external magnetic field 1 mm above the surface of the packaged MAGFET. In order to cancel any external induction effects of the coils, the magnetic source was on-chip at this time. The DUT (MAGFET # 3) was under the influence of a pulsed signal (V_P) with T = 2 s and 10 ns rise/fall times, applied only to the interconnect line # 9 (2.3 Ω); and in doing so, a magnetic flux density (14.60 mT) will be affecting the region.

The conversion from drain current imbalance to drain differential output (V_{out} =$I_{DS1}R_1-I_{DS2}R_2$), was by means of the external resistors (R_1 = R_2 = 994.2 Ω). For illustration, in Fig. 6 the device was capable of detecting two different periodic pulsed voltage signals applied to line #9 by the SPA (voltage mode) (V_P = 1.0 and 1.1 V). The non-linear behavior, when V_P= 0 is just the difference between V_{DD} and V_{DS}. Concluding this preliminary study, in Fig. 7a and 7b we present both drain currents as a time function for MAGFET # 3 without any external influence and under a sinusoidal current (I_{LINE}) applied to the interconnect line, respectively. It is apparent that because of the Lorentz Force a current ($I_{DS}+\Delta I_{DS}$) will be measured in one of the drains whereas another one will sense a current ($I_{DS}-\Delta I_{DS}$). The exponential-like shape of the drain current magnitude reduction as a time function, keeping all the electrical parameters constant, is probably related to a parasitic charge/discharge effect associated to the Si package that requires to be de-embedded from measurements. The intrinsic difference of both currents was on account of the drain width mismatch ($W_1 \neq W_2$).

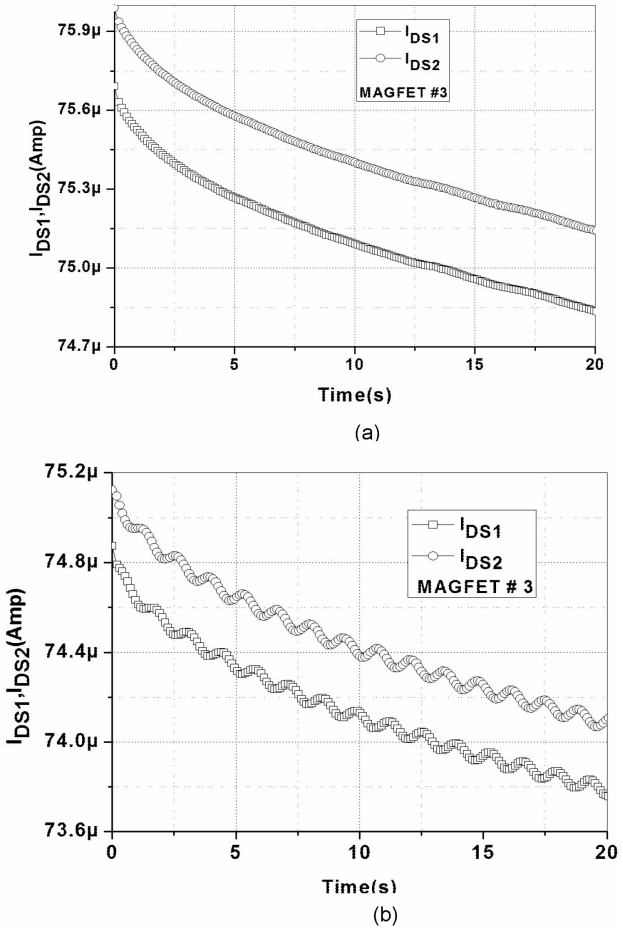

FIGURE 7. Measurement data of both drain currents (I_{DS1} and I_{DS2}) of MAGFET # 3. (a) I_{LINE} = 0, V_{GS} = 5V, V_{DS1} = V_{DS2}= 1V. (b) I_{LINE} = 3.2 mA time-varying sinusoidal current source at 0.9 Hz, V_{GS}= 5V and V_{DS1}= V_{DS2}= 1V.

5. Conclusion

We have experimentally demonstrated that the interconnect current induces an on-chip magnetic flux density. A MAGFET, which is CMOS-compatible, and that can be integrated on the same chip, can be used to monitor both the integrity of the electrical signal on-chip, as well as the magnetic flux density radiation. Having an array of MAGFETs distributed on the surface of the chip would serve to monitor the EM radiation, which in turn may be used for prediction and mitigation of RF interference. For our particular test chip the perpendicular component B_Z generates at a rate of 100 μT/mA, whereas the tangential one B_Y does at a rate of 133 μT/mA. Due to the Lorentz's force, the coupling of B_Z and B_Y with the MOS transistor drain current, induces horizontal and vertical fluctuations of channel charges and mobility. These spatial fluctuations result in corresponding drain current fluctuations ($\Delta I_{DS}/B_Z$)=1.5 μA/mT and ($\Delta I_{DS}/B_Y$) = 0.26 μA/mT. The electro-magnetic ($\Delta I_{DS}/\Delta B$) coupling rate is larger for deeper submicron technologies, which is an indication that on-chip EM interference can get worst for deeper submicron MOS technologies. These results allow establishing the basis for a future development for on-chip magnetic probe for nanometer MOS technologies. The MAGFET could be used for future on-chip applications in the field of telecommunications, multimedia, and consumer electronics domain as on-chip antennas in silicon IC's transmission, alignment-independent chip-to-chip communication for sensors, and wear-free angular positioning control systems.

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