A 1.7 MHz Chua's circuit using VMs and CF+s

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In this paper, a high-frequency Chua's chaotic oscillator based on unity gain cells (UGCs) is introduced. Leveraging the internal buffers of the integrated circuit AD844, a voltage mirror (VM) and a positive current follower (CF+) are designed, taking into account the parasitic elements associated to each UGC. Afterwards, the behavior of the nonlinear resistor and of the grounded inductor are designed by using several VMs, CF+s, discrete capacitors and resistors. In this way, Chua's circuit is built by coupling a nonlinear resistor and an active LC tank circuit by using an RC passive filter. Hspice simulations performed at the state space and in the time and frequency domains show that the proposed topology generates chaos at 1.7 MHz. Experimental results are given, verifying that the chaotic spectrum is extended to high-frequency and showing close agreement with theoretical analysis. The proposed topology is compared with other topologies reported in the literature, showing that a number reduced of active devices and passive elements along with smaller supply voltages can be used to generate chaotic oscillations at high-frequency. Sensitivity and Monte Carlo analysis are also done in order to research the robustness of the proposed chaotic circuit.

Keywords: Chaos; unity-gain cells; chua's circuit; double-scroll; voltage-mirror; current-mirror.

El diseño de un oscilador caótico de Chua basado en celdas de ganancia unitaria y operando en alta frecuencia es presentado. Aprovechando los buffers internos del circuito integrado AD844, un espejo de voltaje y un seguidor de corriente positivo son diseñados, incluyendo los elementos parásitos asociados a cada celda de ganancia unitaria. Posteriormente, el comportamiento de un resistor no lineal y de un inductor aterrizado son realizados usando varios espejos de voltaje, seguidores de corriente, resistores y capacitores discretos. De esta manera, el resistor no-lineal es acoplado a un circuito tanque LC usando un filtro pasivo RC. Resultados de simulación en el plano de fase, en los dominios de tiempo y frecuencia, realizados en Hspice, muestran que la topología propuesta genera formas de onda caóticas a 1.7 MHz. Resultados experimentales son también mostrados a fin de verificar el comportamiento caótico en alta frecuencia y la similitud de los resultados experimentales con el análisis teórico. La topología propuesta se compara con otras topologías reportadas en la literatura, mostrando que un número reducido de dispositivos activos y elementos pasivos junto con voltajes de alimentación más pequeñas, pueden ser usados para generar oscilaciones caóticas en alta frecuencia. Análisis de sensibilidad y de Monte Carlo son realizados con el fin de investigar la robustez del circuito caótico propuesto.

Descriptores: Caos; celdas de ganancia unitaria; espejo de voltage; espejo de corriente.

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1. Introduction

Chaotic dynamical systems have been subject of study since several decades due to their commercial applications in areas like medicine, biology and secure communication systems [1–3]. Particularly in the last issue, chaotic waveforms can be used as modulation and demodulation blocks into a communication system [3]. In this context, chaos generators must not only have a simple design but also the chaotic attractors should operate at high-frequency in order to transmit high-speed data. Among all available chaotic oscillators, Chua's circuit is the most used one since it is an electronic circuit that can easily be built, simulated and tractable mathematically [4–6]. Basically, Chua's circuit is composed by a passive LC tank circuit coupled with a nonlinear resistor (NR) by using an RC passive filter [4]. From the five elements of Chua's circuit, the behavior of the grounded inductor and of the NR have been emulated by using second generation current conveyor (CCII) [1, 7], diodes [2, 8], operational transconductance amplifier (OTA) [4], current feedback operational amplifier (CFOA) [5, 9–12] and operational amplifier (Opamp) [6]. However, despite the advantages on bandwidth, wide dynamic range and high accuracy associated to the active devices, the high-frequency behavior of Chua's circuit must still be improved [13]. For instance, in the first designs of Chua's circuit, Opamps were used to emulate the behavior of either, the NR and/or the grounded inductor [6]. However, due to frequency limitations and non-idealities of the Opamps, most of the proposed topologies in the literature are working in low frequency. In order to increase the operating frequency of Chua's circuit, others active devices (like OTAs, CCIIs and CFOAs) with better characteristics on bandwidth and slew-rate were used to emulate the behavior of the NR and of the grounded inductor [1,4,5,7,9–12]. However, although the frequency performance was improved, the chaotic waveforms are still in the kHz range, with exception of [11, 14] which show chaotic oscillations to few MHz. Furthermore, the behavior of the NR has also been emulated with a tunnel diode and although double-scroll chaotic oscillations in the MHz range have been generated by numerical simulations, a DC voltage source is necessary to bias the tunnel diode [8]. Double-scroll chaotic attractors can also be generated by using negative-gm LC tank oscillators, but the use of large discrete inductors are limiting their operation at high-frequency [15]. Therefore, new design ideas are currently searched to mainly improve the frequency behavior of the NR

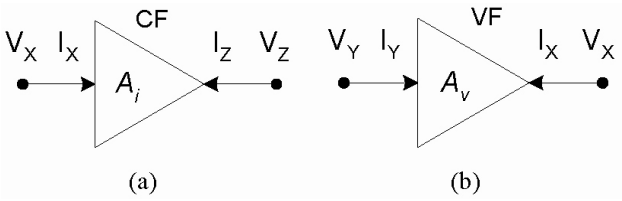


FIGURE 1. (a) Symbol of a CF and (b) Symbol of a VF

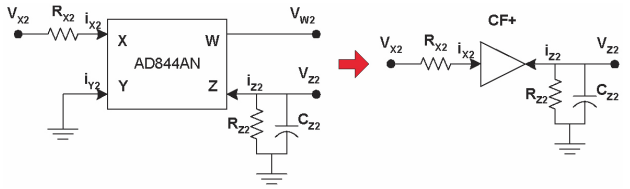


FIGURE 2. CF+ designed with the AD844 and considering parasitic elements

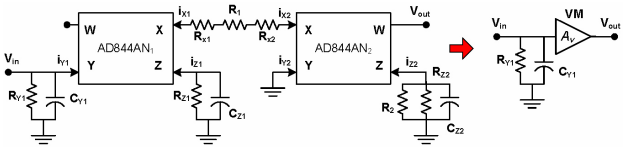


FIGURE 3. VM designed with the AD844 and considering parasitic elements

and of the grounded inductor. As a consequence high-frequency chaotic waveforms from Chua's circuit can be generated.

On the other hand, positive-negative voltage followers (VFs±) and positive-negative current followers (CFs±) are versatile analog building blocks in the analog signal processing, since they have several advantages on wider bandwidth, low-voltage bias, low-power consumption and simpler architectures compared with other more complex active devices [16–18]. Note that a voltage mirror (VM) is also known as VF- or voltage inverter and a CF+ is also known as current mirror. It is worth mentioning that simplest designs will have better performances in speed since they will present less dependence of parasitic elements. Following this idea, Chua's circuit has been designed by using CMOS VFs and CFs, showing its frequency spectrum in the MHz region [14]. Also, the topology introduced in Ref. 13 was experimentally tested in Ref 19, where the UGCs, the grounded inductor and the NR were designed by using the integrated circuit AD844 [20]. However, the operating frequency of Chua's circuit was limited to few kHz.

Henceforth, this paper describes the analysis, design and experimental results of an alternative topology to design Chua's circuit. In particular, a new circuit to design the NR is introduced which uses one VM, two CF+s and four resistors. Later on, the NR is coupled with an LC tank circuit by using an RC filter, where the behavior of the grounded inductor based on UGCs is used [13]. As a consequence, a new Chua's circuit topology based on UGCs is obtained, which can generate chaotic waveforms in the MHz range. Furthermore, the proposed circuit can be used to enhance the chaotic communication system introduced in Ref. 21 and for generating high-frequency multiscroll chaotic attractors, taking into account real parameters of the active devices [7]. To purposes of experimental tests, each UGC is implemented with the AD844, where parasitic elements associated to each terminal of the integrated circuit and of the horizontal connection lines on the breadboard are considered during the design process. The rest of the paper is organized as follows. In Sec. 2, the concept of the VM and CF+ are briefly revised and their implementations by using the AD844 are introduced. The analysis of the NR topology designed with UGCs is described in Sec. 3. Hspice simulations are discussed in Sec. 4. Experimental results, comparisons with other designs reported in the literature and sensitivity results along with Monte Carlo analysis are shown in Sec. 5. Finally the conclusions are given in Sec. 6.

2. Unity-gain cells design

Due to advantages on wider bandwidth, low-power and simpler architectures, UGCs have been used as building basic blocks in the realization of filters [22], oscillators [17, 18] and also on Chua's circuit design [13, 19]. The CF± shown in Fig. 1(a), is characterized by

$$V_X = 0, \quad I_Z = A_i I_X \tag{1}$$

where $A_i = \pm 1$ is the current gain of a CF±, respectively. Also, the VF± shown in Fig. 1(b) is characterized by

$$I_Y = 0, \quad V_X = A_v V_Y \tag{2}$$

where $A_v = \pm 1$ is the voltage gain of a VF and a VM, respectively. Note that a VM is the voltage version of the current mirror [16]. Although UGCs can be designed with CMOS technology [14, 16, 18], herein the VM and CF+ are implemented with the AD844, since it is internally composed by two VFs and one CF+ [20]. According to the internal configuration of the AD844, a CF+ is obtained by grounding the *y*-terminal as shown in Fig. 2 [19]. In order to obtain a VM, one CF+, two VFs and two resistors (labeled as R_1 and R_2) are used, as shown in Fig. 3. Furthermore, the VM can also be obtained by using a CCII- and it can easily be implemented with the AD844. Analyzing Fig. 3, the voltage gain is given by

$$A_v = -\frac{1}{(R_1 + R_{X1} + R_{X2})C_{Z2}\left(s + \frac{1}{R_a C_{Z2}}\right)} \tag{3}$$

where $R_a = R_2 || R_{Z2}$, R_{X1}, R_{X2}, R_{Z2}, and C_{Z2} are the parasitic resistors and capacitors associated to the *x*-terminal and *z*-terminal of each AD844, respectively. According to (3), the dominant pole of the VM is given by $1/(R_a C_{Z2})$. From Fig. 3 one can see that if the VM is analyzed separately, the parasitic elements associated to the *y*-terminal of the $AD844_1$

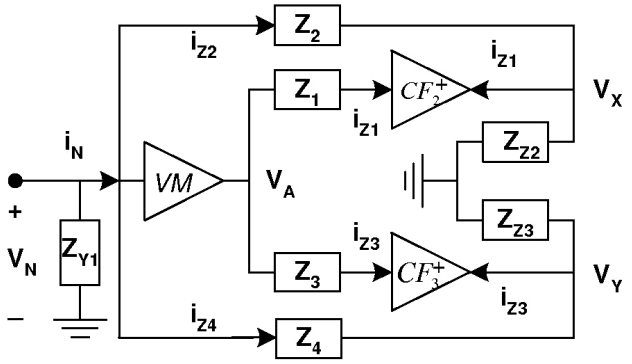


FIGURE 4. NR by using one VM and two CF+s

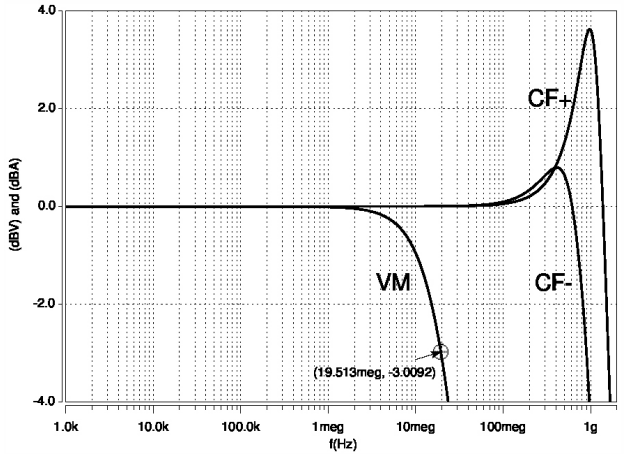


FIGURE 5. Hspice results of the frequency response of the VM, CF- and CF+

and given by R_{Y1} and C_{Y1} do not influence in (3), but however, these parasitic elements become important when the VM is used into an analog system, as will be illustrated in Sec. 4.

3. NR with VMs and CF+s

Chua's circuit has been designed with UGCs [13] and it has been experimentally tested in Ref. 19, showing well behavior at low frequency. According to the proposed topology in Ref. 13, the CF- is built by using two AD844 and the VF with one AD844. Therefore, five integrated circuits are needed to design the NR. On the other hand, the proposed NR topology use two AD844 to design the VM, one AD844 to each CF+ and four resistors, as shown in Fig. 4. By considering parasitic elements it can easily be shown that V_X and V_Y from Fig. 4, are given as

$$V_X = \frac{V_N Z_{Z2}(Z_1 + Z_2 A_v)}{Z_1(Z_{Z2} + Z_2)} \approx V_N \left(\frac{Z_2 A_v}{Z_1} + 1 \right) \quad (4)$$

$$V_Y = \frac{V_N Z_{Z3}(Z_3 + Z_4 A_v)}{Z_3(Z_{Z3} + Z_4)} \approx V_N \left(\frac{Z_4 A_v}{Z_3} + 1 \right) \quad (5)$$

The currents flowing throught Z_2 and Z_4 are given as

$$i_{Z_2} = \frac{1}{Z_2}(V_N - V_X), \quad i_{Z_4} = \frac{1}{Z_4}(V_N - V_Y) \quad (6)$$

where

$$Z_1 = R_1 + R_{X2} \quad Z_2 = R_2$$
$$Z_3 = R_3 + R_{X3} \quad Z_4 = R_4$$
$$Z_{Z2} = R_{Z2}||C_{Z2} \quad Z_{Z3} = R_{Z3}||C_{Z3}$$
$$Z_{Y1} = R_{Y1}||C_{Y1}$$

The output current signal of a CF+ is restricted by the dynamic range associated to the current mirrors into the AD844 (*i.e.* at the *z*-terminal). Therefore, the output current will work almost linear until a maximum output current, before that the input current achieves to saturate the current mirrors. In fact, the input current of the CF+s is controlled by V_A/Z_1 and V_A/Z_3, respectively, where V_A is the output voltage from VM. Thus, V_X and V_Y are reaching positive-negative saturation regions at $\pm E^{\pm \text{sat}}$ and hence, the breakpoints are achieved. This way, by considering parasitic elements and following the analysis given in Ref. 13, the slopes and breakpoints of the NR are given as

$$\begin{aligned}
m_0 &= \frac{1}{Z_2} + \frac{1}{Z_4} \\
m_1 &= \frac{1}{Z_4} + \frac{Z_3 - Z_{Z3}A_v}{Z_3(Z_{Z3} + Z_4)} \approx \frac{1}{Z_4} - \frac{A_v}{Z_3} \\
m_2 &= \frac{Z_1 - Z_{Z2}A_v}{Z_1(Z_{Z2} + Z_2)} \\
&\quad + \frac{Z_3 - Z_{Z3}A_v}{Z_3(Z_{Z3} + Z_4)} \approx -A_v \left(\frac{1}{Z_1} + \frac{1}{Z_3} \right) \qquad (7) \\
\pm E_1 &= \pm \frac{E_{sat}^{\pm} Z_3(Z_{Z3} + Z_4)}{Z_{Z3}(Z_3 + Z_4 A_v)} \\
&\approx \pm \frac{E_{sat}^{\pm}}{1 + \frac{Z_4 A_v}{Z_3}} \pm E_3 = \pm E_{sat}^{\pm} \\
\pm E_2 &= \pm \frac{E_{sat}^{\pm} Z_1(Z_{Z2} + Z_2)}{Z_{Z2}(Z_1 + Z_2 A_v)} \approx \pm \frac{E_{sat}^{\pm}}{1 + \frac{Z_2 A_v}{Z_1}} \qquad (8)
\end{aligned}$$

Equations (7) and (8) are less dependent of parasitic elements compared with those equations given in Ref. 19 and as a consequence, the new NR topology will perform a better performance at high-frequency. However, there is a limit on the operating frequency of the NR, which is governed by the behavior at frequency of the VM. From Fig. 4 one can see that $Z_{Y1} = R_{Y1}||C_{Y1}$ (see Fig. 3) does not influence in (7) and (8), but however, Z_{Y1} becomes important during the chaotic oscillator design, as will be illustrated in next section.

4. Hspice simulations

Waveforms of a chaotic oscillator are nearly sinusoidal when the output power is concentrated in a single-frequency com-

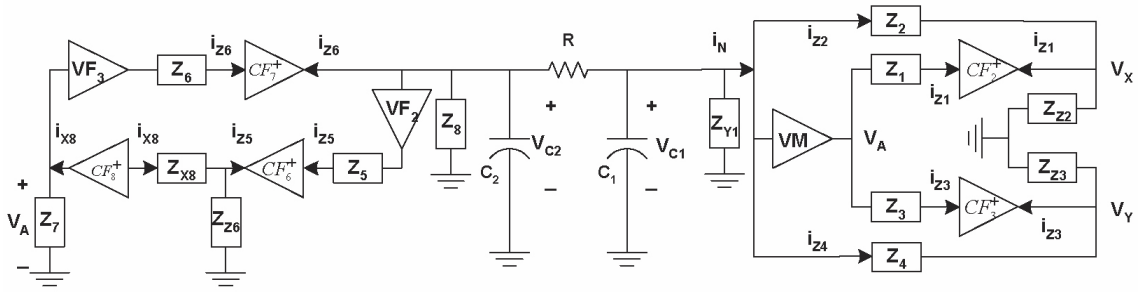


FIGURE 6. Chua's circuit employing UGCs

ponent which is centered near the operating frequency of the active LC tank circuit. On the other hand, the waveforms become chaotic if the circuit is tuned in its chaotic region of operation by varying any of its elements. Thus, the power is spread to more frequency components both higher and lower than the center frequency of oscillation. However, to achieve high-frequency chaotic oscillations, the NR must have well performance in the operating frequency of the LC tank circuit. Because the NR shown in Fig. 4 is based on UGCs, we investigate the frequency response of the VM shown in Fig. 3, CF+ shown in Fig. 2 and CF- designed with two CF+ connected in series. Typical values of the parasitic elements associated to each terminal of the AD844 are: R_Y=10 MΩ, R_X=50 Ω, R_Z=3 MΩ, C_Y=2 pF, C_Z=4.5 pF [20]. For the VM design, R_1=1.55 kΩ and R_2=1.6 kΩ are used to minimize the effect of the parasitic resistance at the *x*-terminal of the AD844. From (3), the dominant pole is computed as 22.11 MHz and it is confirmed by numerical simulations depicted in Fig. 5. Hspice simulations of the CF±s are also shown in Fig. 5. Furthermore, the VM will limit the frequency performance of the NR since its gain is less of 0 dB at 2 MHz. With this constraint in mind, we propose a novel topology of Chua's circuit in order to generate chaotic waveforms at high-frequency, as shown in Fig. 6. In this circuit, we can identify to Z_{Y1} (*i.e.* the parasitic elements of the VM) connected in parallel with C_1. Similarly, the parasitic elements of the VF_2 (*i.e.* R_{Y2} and C_{Y2}) and of the CF_7^+ (*i.e.* R_{Z7} and C_{Z7}) are all connected in parallel and labeled by $Z_8 = R_{Y2}||R_{Z7}||(C_{Y2} + C_{Z7})$. Further, Z_8 and C_2 are also connected in parallel. In order to get total control on the generation of chaotic waveforms at high-frequency, Z_{Y1} and Z_8 impose a low limit on the numerical value of $C_1 > C_{Y1}$ and $C_2 > C_{Y2} + C_{Z7}$. Contrary, the behavior of the chaotic system at high-frequency is governed by the parasitic capacitors. The analysis of the grounded inductor designed with UGCs is described in Ref. 13. Therefore, by using (3)-(8) along with all considerations described above, the behavior of Chua's chaotic oscillator based on UGCs is achieved. Hspice simulation results of a double scroll attractor is shown in Fig. 7(a) and the waveforms in the time domain are depicted in Fig. 7(b), where: R_1=2.2 kΩ, R_2=1 kΩ, R_3=180 Ω and R_4=2.8 kΩ are used to design the NR; R_5=820 Ω, R_6=1 kΩ and C_7=4.7 pF are used to get L=8.4 μH; C_1=2 pF, C_2=8 pF and R =810 Ω along with the NR and the grounded active inductor previously described are used to design the chaotic oscillator. For all the UGCs, the AD844 macro-model was biased with ±5 V.

5. Experimental results

The proposed chaotic oscillator shown in Fig. 6 was tested on a breadboard by using discrete components with the same values used in simulation, but with mild modifications. Thus, Chua's circuit was tuned at frequency by modifying: R = 390 Ω, R_4=22 kΩ and C_7=47 pF. Figure 8(a) shows experimental results corresponding to $V_{C2} - V_{C1}$ projection of the trajectories and the dynamic behavior in the time domain is shown in Fig. 8(b). On the other hand, when the chaotic signal from Chua's circuit is almost sinusoidal, the output power is concentrated near the operating frequency of the active LC tank circuit. In this context, Fig. 9(a) shows the center frequency of oscillation of the LC tank circuit which is centered approximately at 1.7 MHz. Later on, Chua's circuit is tuned towards its chaotic region of operation by varying R, as shown in Fig. 9(b), confirming the theory and numerical simulations. Because Chua's circuit was tested on a breadboard, the parasitic capacitance among several horizontal connection lines of the breadboard was previously measured. According to Fig. 10(a), the parasitic capacitance between two adjacent lines is 2.7 pF and this decreases when the distance between lines increases. In order to minimize the effect of the parasitic capacitances of the breadboard on the proposed topology shown in Fig. 6, the discrete passive elements were connected at least 5 lines of separation. For instance, in Fig. 6, C_1 is connected on the breadboard by leaving 5 connection lines as separation among its terminals. Therefore, from Fig. 10(a) and taking into account the parasitic capacitance C_{Y1} from VM and C_1, the total capacitance across C_1 is approximately 5 pF. A picture of the physical circuit is shown in Fig. 10(b). Furthermore, the proposed topology is compared with several topologies reported in the literature in terms of the kind of active device used to emulate the behavior of Chua's diode and the grounded inductor, the chaotic frequency spectrum, supply voltages and experimental measurements, as summarized in Table I. Therefore, we can see that [8, 11, 14] report simulation results of chaotic waveforms operating in the MHz region, whereas numerical and experimental results are reported herein. However, al-

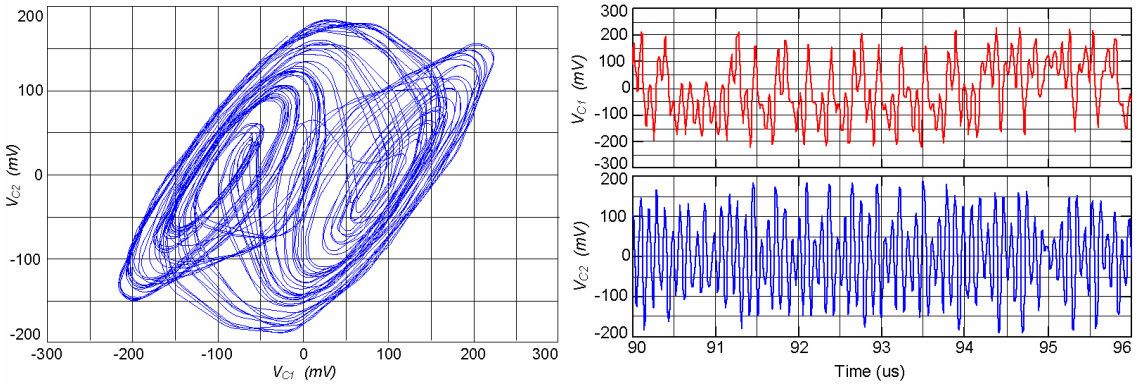


FIGURE 7. Hspice simulation results (a) $V_{C2} - V_{C1}$ projection (b) Waveforms in the time domain

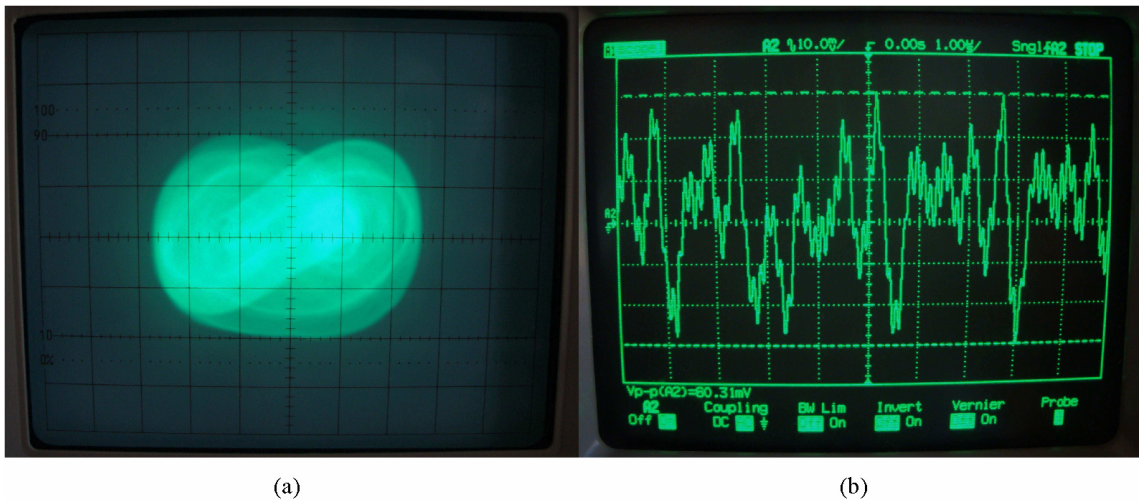


FIGURE 8. (a) The double scroll attractor experimental. Vertical axes: V_{C2} (20 mV/div), Horizontal axes: V_{C1} (20 mV/div) (b) Experimental results in the time domain

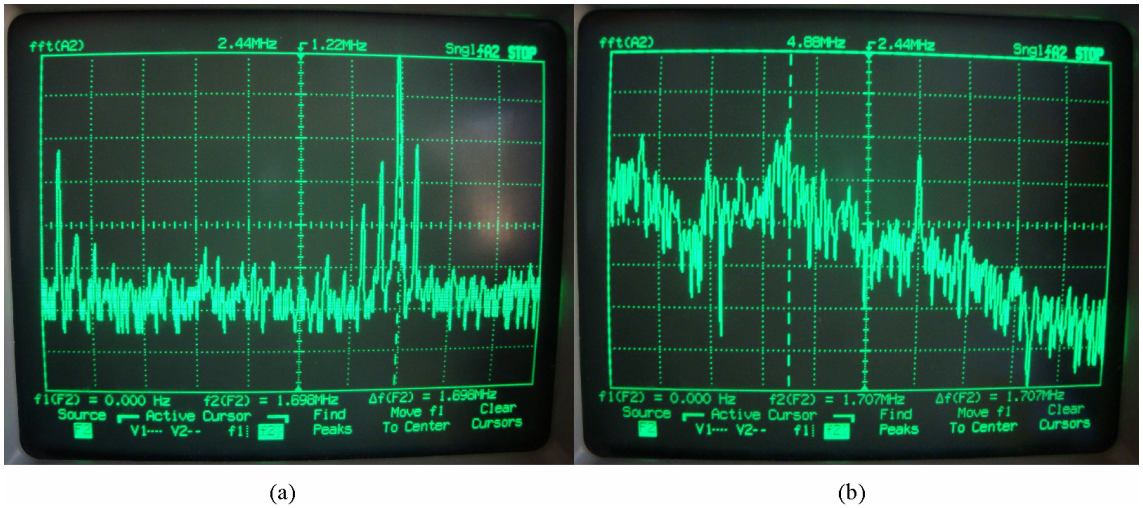


FIGURE 9. (a) Frequency spectrum of the active LC tank circuit, (b) Experimental measurement of the chaotic spectrum

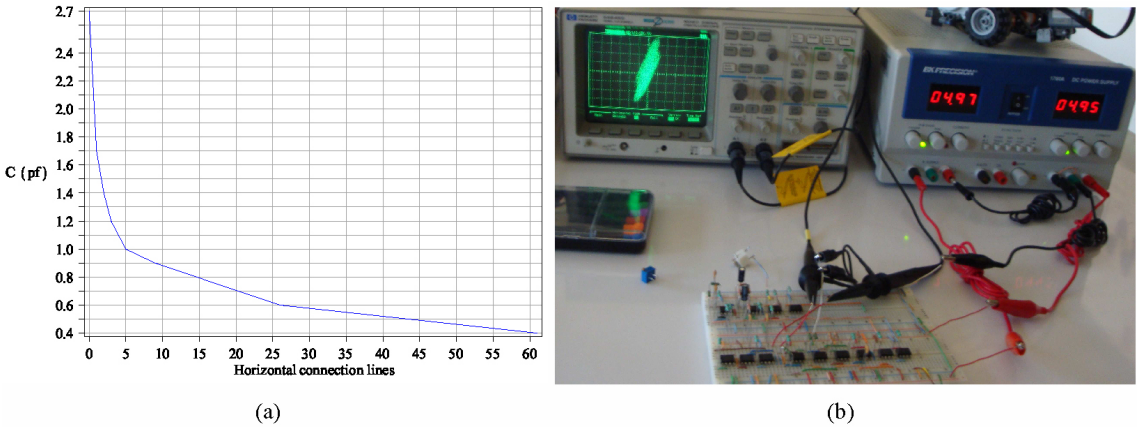
TABLE I. Comparison of Chua's circuit designed with different active devices

Chua's diode based on	Grounded inductor based on	Chaotic frequency spectrum	Bias (Volts)	Experimental results	Reference
Opamp	discrete inductor (L=18 mH)	≈3.7 kHz	±9	Yes	[6]
CFOA	CFOA	≈4.2 kHz	±15, ±11.23, ±4.05	Yes	[9]
CFOA	discrete inductor (L=120 μH)	522 kHz	±9	Yes	[5]
Tunnel diode	discrete inductor (L=10.68 nH)	30 MHz	0.3117 (To bias the tunnel diode)	No	[8]
Opamp	CFOA	20.2 kHz	±9	Yes	[10]
Opamp	Opamp	≈3.5 kHz	±15	Yes	[2]
CFOA	CFOA	2.25 MHz	±9	No	[11]
CCII	CCII	37.5 kHz	±7.8	No	[1]
UGCs	UGCs	2.5 MHz	±1.5	No	[14]
UGCs	UGCs	≈2.3 kHz	±5	Yes	[19]
CFOA	CFOA	100 kHz	±10	Yes	[12]
UGCs	UGCs	1.7 MHz	±5	Yes	This work

TABLE II. Sensitivity analysis of the VM, NR, Chua's circuit and supply voltages

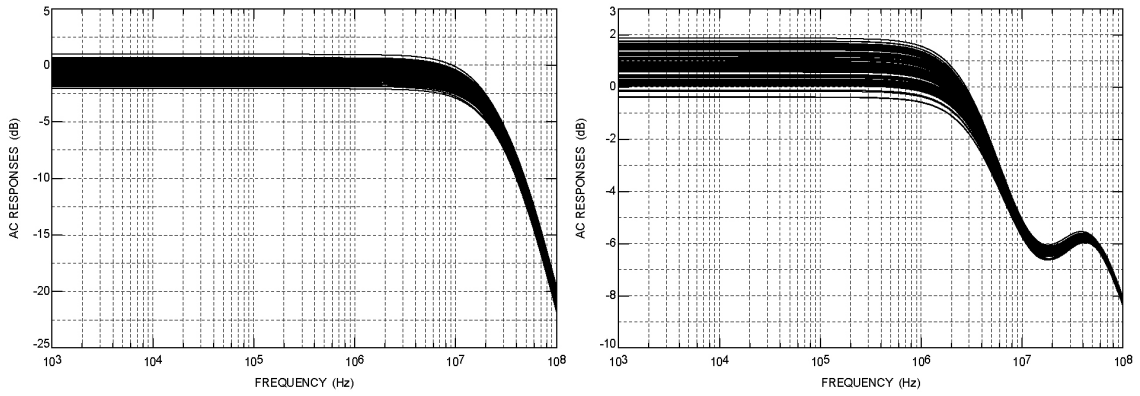
Topology	Element name	Element value	Element sensitivity (volts/unit)	Normalized sensitivity (volts/percent)
Fig. 3	R_1	1.55 kΩ	-6.223e-09	9.646e-08
	R_2	1.6 kΩ	-1.935e-07	-3.097e-06
Fig. 4	R_1	2.2 kΩ	-1.894e-08	-4.167e-07
	R_2	1 kΩ	-4.461e-11	-4.461e-10
	R_3	180 Ω	-1.814e-06	-3.266e-06
	R_4	2.8 kΩ	-1.782e-10	-4.989e-09
	R_1 (VM)	1.55 kΩ	-7.765e-07	-1.204e-05
	R_2 (VM)	1.6 kΩ	3.816e-07	6.106e-06
Fig. 6	R	810 Ω	-1.471e-10	-1.192e-09
	R_1 (Ind.)	1 kΩ	-2e-07	-2e-06
	R_2 (Ind.)	820 Ω	-9.745e-11	-7.991e-10
	R_1 (NR)	2.2 kΩ	-1.161e-13	-2.555e-12
	R_2 (NR)	1 kΩ	-8.076e-15	-8.076e-14
	R_3 (NR)	180 Ω	-1.112e-11	-2.002e-11
	R_4 (NR)	2.8 kΩ	-8.885e-15	-2.488e-13
	R_1 (VM)	1.55 kΩ	-1.291e-10	-2.001e-09
	R_2 (VM)	1.6 kΩ	2.196e-11	3.514e-10
Supply voltages	V_{cc}	+5V	1.734e-04	8.67e-06
	V_{ee}	-5V	1.734e-04	-8.67e-06

though [8] shows chaotic waveforms at high-frequency, a tunnel diode along with a DC voltage source are necessary to emulate the Chua's diode. In Ref. 11, the chaotic frequency spectrum of 2.25 MHz by using power supply voltages of ±9 V is reported, whereas in Ref. 14 the chaotic spectrum is extended to 2.5 MHz by using ±1.5 V to bias the UGCs. Otherwise, this paper shows experimental results of chaotic waveforms from Chua's circuit operating at high-frequency and by using ±5 V as power supply voltages. It is worth mentioning that in Ref. 15, a third order dynamic system is used to generate numerically double scroll attractors operating in the GHz range. Nonetheless, the experimental tests show that the operating frequency is into the MHz range. Furthermore, [15] is not included in Table I because the dynamic system used is different of Chua's system.



(a) (b)

FIGURE 10. (a) Parasitic capacitance among horizontal connection lines of a breadboard (b) The physical circuit.



(a) (b)

FIGURE 11. Monte Carlo analysis of the (a) VM and (b) Nonlinear resistor.

An important feature in the design of any system is its robustness, which depends on the sensitivity of the components. In this context, a DC small-signal sensitivity analysis of the VM shown in Fig. 3, NR depicted in Fig. 4 and Chua's circuit shown in Fig. 6 with respect to variations of the passive resistors and the supply voltages were done. Sensitivity analysis was performed on Hspice and the results are reported in Table II. For the VM, the results were measured on the output terminal, whereas the NR was connected in series with a 454 Ω resistor and the results were computed across the NR. Sensitivity results of Chua's circuit were measured across C_2. Because Chua's circuit is a nonlinear system, Monte Carlo simulations of the most critical cells were also done on Hspice simulator. Thus, Fig. 11 shows numerical results of the VM and NR respectively, where the values of passive components were varied randomly using a relative Gaussian distribution with 5% of tolerance on the nominal values. According to Table II, one can conclude that the proposed topology is robust in small variations of the passive componentes and near the operating point. However, this property gets lost in large variations. Furthermore, among all pasive components from Fig. 6 and Fig. 3, R, R_1 and R_2 are the most sensitive elements and they are conditioning the robustness of the proposed circuit. After several experimental tests, it is concluded that the parasitic elements of the grounded inductor, NR and of the breadboard, play a role important at the high-frequency performance of the proposed chaotic oscillator. Further, among all the UGCs previously designed, the VM is the most critical cell with respect to the frequency performance, since the bandwidth is extended to few MHz as shown in Fig. 5. Therefore, higher frequency chaotic oscillations can be achieved by designing the UGCs with CMOS technology.

6. Conclusions

A novel topology of Chua's circuit based on UGCs has been introduced. Basically, the behavior of the grounded inductor and of the NR was modeled by using UGCs and each of them was designed by using the integrated circuit AD844, where parasitic elements associated to the input-output terminals of the AD844 were considered. Particularly, the NR based on UGCs has been improved, since the breakpoints and slopes are less dependent of parasitic resistors and capacitors, compared with that introduced in Ref. 19. As a consequence, chaotic oscillations were achieved to 1.7 MHz. Hspice sim-

ulations along with experimental results in the time domain and state space were shown in order to illustrate the capability of the proposed topology. Comparisons among this work and those reported in the literature were also introduced. Furthermore, sensitivity and Monte Carlo analysis were done in order to research the robustness of the proposed topology.

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