# Electrical characterization of planarized a-SiGe:H Thin-film Transistors

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Recibido el 25 de julio de 2012; aceptado el 22 de octubre de 2012

In this work the electrical characterization of n-channel a-SiGe:H TFTs with planarized gate electrode is presented. The planarized a-SiGe:H TFTs were fabricated at 200°C on corning glass substrate. The devices exhibit a subthreshold slope of 0.56 V/Decade, an on/off-current ratio approximately of $10^6$ and off-current approximately of $0.3\times10^{-12}$ A. The results show an improvement of the electrical characteristics when are compared to those unplanarized devices fabricated at higher temperature. Moreover, the simulation of the device using a SPICE model is presented.

*Keywords:* Thin-film transistor; hydrogenated amorphous silicon–germanium; low-temperature; spin-on glass; spice.

PACS: 81.05.Gc; 81.15.Gh; 85.30.Tv

## 1. Introduction

Electronic devices fabricated on flexible and large-area substrates are the subjects of growing attention within the research community. Thin-film transistors (TFTs) based on a-Si:H technology have attracted interest due to potential low-temperature process to be integrated in flexible electronics technology. Also, this technology offers the advantage of materials science, device physics and equipment which are already well established.

In the a-Si:H technology, the gate insulator is usually based on plasma deposited silicon nitride (SiNx) [1]. However, the reduction of its deposition temperature in order to make it compatible with flexible plastic substrates often leads to a material with poor dielectric performance. At deposition temperatures below 300°C, the leakage current through SiNx films increases rapidly due to low film mass density [2,3]. Thus, the low-temperature gate insulator material must have good insulating properties and low charge-trapping rate at low electric fields, and should form a high-quality interface with the a-Si:H semiconductor layer (insulator-semiconductor interface). In this topic, silicon oxide films ($SiO_2$) deposited by Spin-On Glass (SOG) at low temperatures results very attractive. Recently, we have studied the properties of $SiO_2$ films from SOG diluted with $H_2O$ and cured at 200°C using conventional equipment for a-Si:H technology [4].

In previous work, we have obtained a-SiGe:H films by low frequency plasma enhanced chemical vapor deposition (PECVD) at 300°C, which have been used as active layer for Thin-film Transistors [5,6]. The fabricated devices, n-channel a-SiGe:H TFTs resulted with a subthreshold slope of 0.9 V/DEC and on/off-current ratio of $10^3$. However, an on/off-current ratio larger of $10^3$ and subthreshold slopes lower than 0.9 V/DEC are required in order to get a good quality switch TFT performance. In this work the electrical characterization of n-channel a-SiGe:H TFTs fabricated at 200°C with planarized gate electrode is presented. Moreover, the simulation of the device using a SPICE model is presented.

## 2. Experiment

The low-temperature a-SiGe:H TFTs used the inverted staggered structure and were fabricated on corning 1737 substrates. The process flow and cross section of the a-SiGe:H TFTs are shown in Fig. 1. The simplified process flow is as follows: first, to planarize the gate electrode, 100 nm-thick of SOG diluted with $H_2O$ and cured at 200°C was used [4]. Then, photoresist was applied and patterned to leave opening for the gate. Later, the SOG was etched by Reactive Ion Etching (RIE) leaving the place of the gate. The SOG was etched with $CF_4$ plasma at a pressure of 160 mTorr and RF power of 50 Watts. Finally, as shows Fig. 1a, the planarized gate is formed by lift-off process of 100 nm-thick of e-gun evaporated Al. Afterwards, 80 nm-thick of SOG diluted with $H_2O$ and cured at 200°C was used as the gate insulator. Then, 100 nm-thick of undoped a-SiGe:H and 100 nm-thick of SiNx films were deposited using low frequency (110 kHz) PECVD at 200°C, pressure of 0.6 Torr and an RF power of 300 W (Fig. 1b). Later, the SiNx film was patterned as passivation layer above the a-SiGe:H active layer using RIE. In this step, an overetching in the a-SiGe:H film was done by RIE as shown in the Fig. 1c. The time of the overetching was of 30 seconds (20% of the a-SiGe:H film thickness). After that, hydrogen plasma was done at 200°C, with $H_2$ flow of 3500 sccm, pressure of 0.6 Torr and RF power of 300 W for

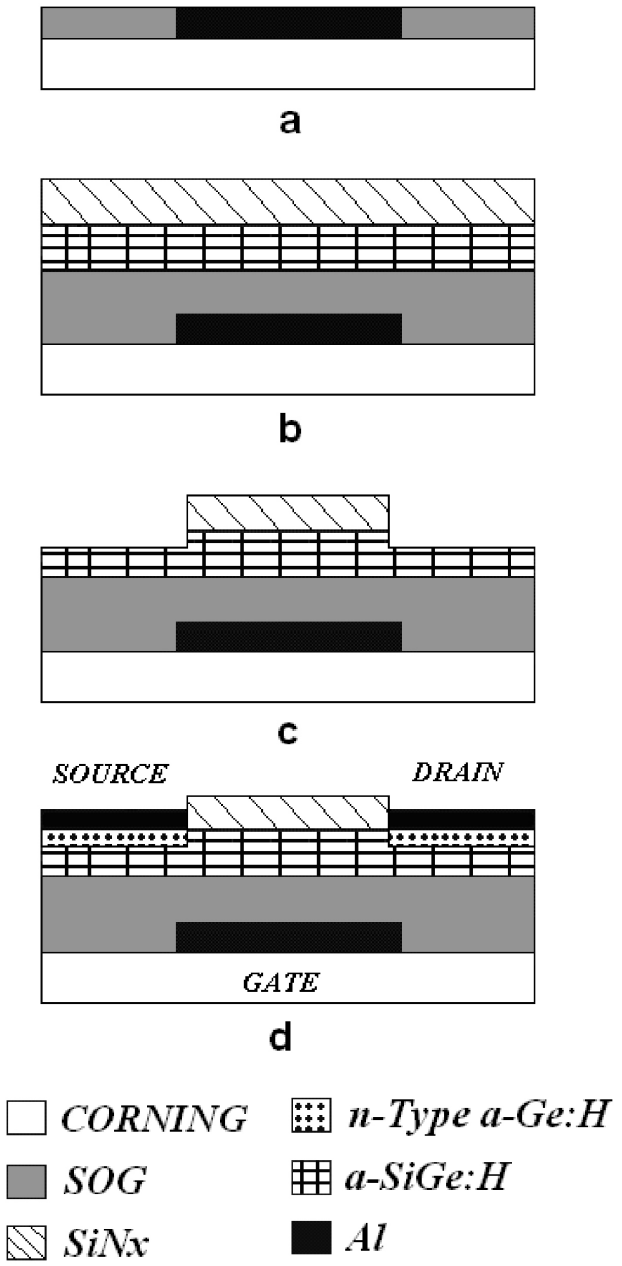


FIGURE 1. Process flow and cross section of the planarized a-SiGe:H TFTs (not to scale).

5 minutes. Next, 40 nm-thick of n-type a-Ge:H film was deposited using low frequency PECVD at 200°C with a pressure of 0.6 Torr and RF power of 300 W. Then, 300 nm-thick of Aluminum was e-gun evaporated and patterned to form the source and drain electrodes. After, the n-type a-Ge:H film was etched using RIE (Fig. 1d). Finally, a thermal treatment at 180°C for 40 minutes was done.

## 3. Results and discussion

The electrical characterization of the devices was conducted using the *HP 4156B Semiconductor Parameter Analyzer*. All the measurements were done under dark conditions. The

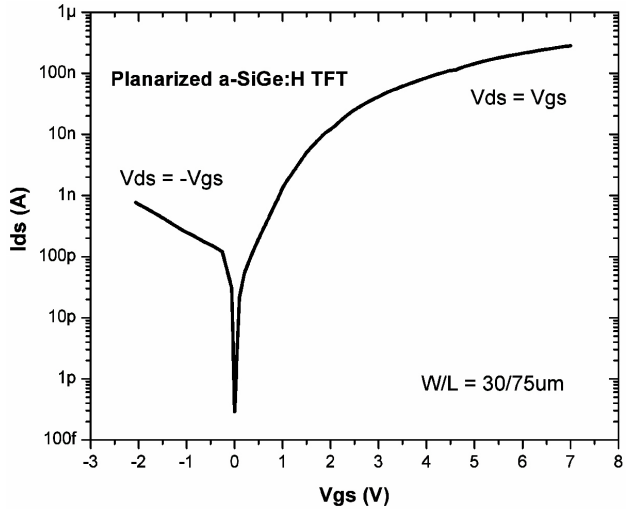


FIGURE 2. Transfer characteristics of the planarized a-SiGe:H TFTs.

transfer characteristics of the planarized a-SiGe:H TFTs is shown in Fig. 2. It can be observed an on/off-current ratio approximately of $10^6$ and an off-current approximately of $0.3\times10^{-12}$ A at 0 Vgs which are in the range of those in high-temperature a-Si:H TFTs and are better than those of the a-SiGe:H TFTs fabricated at 300°C, previously reported [6]. The subthreshold slope of the a-SiGe:H TFT was 0.56 V/DEC. Typically, in a-Si:H TFTs, the subthreshold slope is largely decided by the quality of gate insulator/ active layer interface. In the a-SiGe:H TFT, the subthreshold slope is dependent on the trap density in the active layer a-SiGe:H ($N_T$) and at the SOG/a-SiGe:H interface ($D_{it}$). The subthreshold slope can be approximated as the following equation [7]:

$$S = qK_BT(N_Tts + D_{\rm it})/C_{\rm ox}\log(e) \qquad (1)$$

Where $q$ is the electron charge, $K_B$ is the Boltzmann constant, T is the absolute temperature, ts is the a-SiGe:H thickness and $C_{ox}$ is the SOG insulator capacitance per unit area. If $N_T$ or $D_{it}$ is separately set to zero, the respective maximum values of $N_T$ and $D_{it}$ are obtained. The $N_T$ and $D_{it}$ values for the planarized a-SiGe:H TFTs were of $2.65\times10^{17}$ cm$^{-3}$eV$^{-1}$ and $2.65\times10^{12}$ cm$^{-2}$eV$^{-1}$, respectively. Figure 3 shows the output characteristics of the a-SiGe:H TFTs. From the above results, we may say that the electrical performance of the planarized a-SiGe:H TFTs fabricated at 200°C was improved respect to the unplanarized a-SiGe:H TFTs fabricated at 300°C. The results obtained are comparable to those of a-Si:H TFTs using SiNx as gate insulator at higher temperatures of fabrication and even better than those reported in polysilicon TFTs using SOG as gate insulator at a maximum temperature of fabrication of 590°C [8,9].

On the other hand, the density of states can be determined from the analysis of the transfer characteristic. However, it is usual to make the assumption that the density of states is

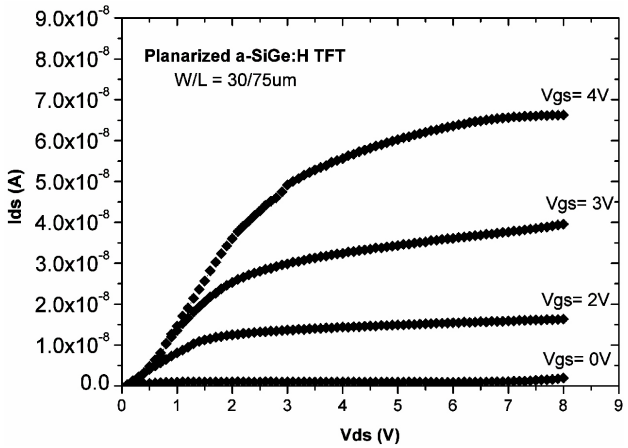


FIGURE 3. Output characteristics of the planarized a-SiGe:H TFTs.

TABLE I. Parameters of Planarized a-SiGe:H TFTs

| Parameter | Value |
|---|---|
| $V_T$ | 1.12 V |
| Vfb | 0.18 V |
| $E_{A2}$ | 30 meV |

homogeneous throughout the active layer and that there are no surface states [10]. In reality, there is some evidence that the DOS is not homogeneous. Therefore, the derived DOS reflects contributions from interfaces. Since the problem of calculating the DOS is enormously difficult, in the sake of simplicity, it was used the method proposed by B. Wu *et al* [11] to obtain the characteristic energies for the deep localized states of the a-SiGe:H film, the flat-band voltage and $V_T$ among other device parameters for the a-SiGe:H TFTs. Table I summarizes results of the electrical measurements.

As far as we know, since in literature there is no existence either physical nor SPICE models of a-SiGe:H TFTs, we use a typical SPICE model used in a-Si:H TFTs because is the most similar in behavior of our TFTs. The a-Si:H TFT model used was the presented by M. Shur *et al.* in Ref. 12. This model has been implemented in AIM-SPICE [13]. The details of the a-Si:H TFT model are presented in Ref. 14. From the electrical characterization of the a-SiGe:H TFTs some material and device parameters were obtained, such as the maximum trap density ($N_T$) and the characteristic energy of the deep states of the a-SiGe:H active layer, besides the threshold voltage $V_T$ and flat-band voltage of the devices.

In a-Si:H films, the typical value of minimum density of deep states $g_0$ is $1\times10^{23}$ $m^{-3}eV^{-1}$ [12,14]. Since the electrical characterization of the planarized a-SiGe:H TFTs showed a relatively higher DOS due to the incorporation of germanium, the value of $g_0$ used to simulate the a-SiGe:H TFTs was higher than that in a-Si:H TFTs but lower than the maximum trap density ($N_T$) in the a-SiGe:H film ($2.65\times10^{17}$ $cm^{-3}eV^{-1}$ or $2.65\times10^{23}$ $m^{-3}eV^{-1}$). The value of $g_0$ was of $1.9\times10^{23}$ $m^{-3}eV^{-1}$ and was corroborated by the agreement of the simulated with the experimental data.

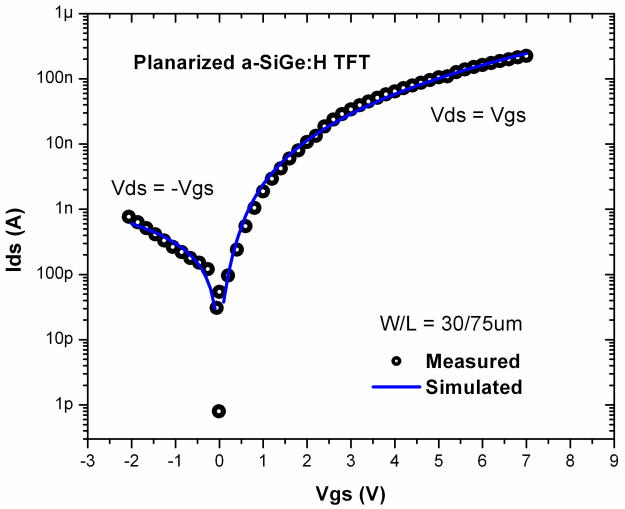


FIGURE 4. Transfer characteristics measured and simulated for the planarized a-SiGe:H TFTs.

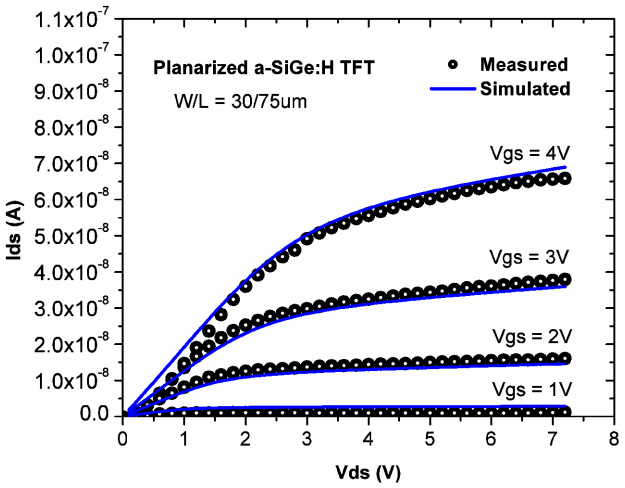


FIGURE 5. Output characteristics measured and simulated for the planarized a-SiGe:H TFTs.

An exponential dependence of the deep states, $g(E) = g_0 \exp[(E - E_{F0})/E_{DD}]$, has been demonstrated in the subthreshold region where the deep states have a strong influence. $E_{DD}$ is the characteristic energy of the deep states and its typical value is $\sim$120 meV [12,14]. The electrical characterization of the planarized a-SiGe:H TFTs showed a characteristic energy of 30 meV (acceptor-deep states). The characteristic energy is lower than those presented in a-Si:H films because the a-SiGe:H film has a higher DOS due to the incorporation of Ge. However, the agreement of the simulated with the experimental data was obtained with a characteristic energy of 40 meV.

The value of the mobility band ($\mu_n$) used in the SPICE model was of 30 $cm^2$/Vs, while the threshold voltage $V_T$ was the extracted in the electrical characterization of the TFT. The other parameters were $V_{AA} = 16\times10^3$ V and $\gamma = 0.6$, both of them in the range of those in a-Si:H TFTs [12,14].

Figure 4 shows the transfer characteristic measured and simulated for the planarized a-SiGe:H TFTs. It is demon-

strated the agreement between the simulated and the experimental data of the planarized a-SiGe:H TFTs. The simulated transfer characteristic agrees very well with the measured data. The same parameter set, also results in accurate description of the output characteristics as shown in Fig. 5. The SPICE model successfully reproduces both measured transfer and output characteristics over a wide range of Vgs and Vds voltages.

## 4. Conclusions

The electrical characterization of n-channel a-SiGe:H TFTs with planarized gate electrode was presented. From the results, the electrical performance of the planarized a-SiGe:H TFTs fabricated at 200°C was improved respect to the unplanarized a-SiGe:H TFTs fabricated at 300°C, previously reported. The results obtained are in the range of those reported in high-temperature a-Si:H TFTs. It was demonstrated the agreement between the SPICE simulated and the experimental data of the planarized a-SiGe:H TFTs over a wide range of Vgs and Vds voltages.

## Acknowledgments

The authors want to thank to all personnel of the laboratory of microelectronics at INAOE and to the CONACYT for the scholarship No. 160547.

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