Common-source cold-FET used to validate noise figure measurements and on-wafer FET noise parameters

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This work proposes the use of a common-source cold-FET with gate forward biased to validate the noise figure measurements and the noise parameters of on-wafer transistors. Since a common-source cold-FET behaves as an attenuator, its noise figure and noise parameters can be determined from S-parameters measurements. Three methods for determining the noise parameters of the common-source cold-FET are investigated. The first one uses the noise correlation matrix for passive devices (the S-parameters), the second one is the tuner method and the third one is the F_{50} method. The noise figure measured and the noise figure computed from S-parameters agree quite well. The noise parameters extracted with the tuner method and the F_{50} method show good correlation with the noise parameters computed with the S-parameters. These results validate both the noise figure measurements and the noise parameters extraction.

Keywords: Noise figure; noise parameters; cold-FET; source-pull tuner method; F_{50} method.

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1. Introduction

Noise figure is one of the receiver parameters; that indicates its ability to process low-level signals. This figure of merit is mainly dictated by the low noise amplifier (LNA), and it depends on the transistors' noise parameters [1,2]. The knowledge of noise figure at different input impedances allows the determination of the four noise parameters (NPs) [3]: minimum noise figure, F_{min}, noise resistance R_n, and the magnitude and phase of the optimum reflection coefficient, Γ_{opt} (or the real and the imaginary parts of optimum admittance, $Y_{opt=}G_{opt}+jB_{opt}$). The NPs depend on both the frequency and the bias point.

The transistor NPs can be determined by using either the multiple-impedance technique (tuner method) [4-8] or the F_{50} method [9,10]. The tuner method uses measures of noise figure at different impedances presented at the input of the device under test (DUT). This technique can be applied to any two-port device. The F_{50} method requires the knowledge of the transistor noise model, and only needs measurements of the transistor noise figure when its input is loaded with a broadband load near 50 ohms. To minimize errors in the noise parameters extraction the F_{50} method uses frequency redundancy. Therefore, errors in the measurements of noise figure and reflection coefficient preclude the correct determination of the NPs. Therefore, high reliable measurements of noise figure and reflection coefficients are required. In this sense, noise verification standards are also sought after in order to validate the noise figure measurements of mismatched devices.

The common-gate cold-FET configuration has been proposed as a verification standard to check the accuracy of NPs [11-12]. The cold-FET in common-gate configuration can be used as a noise verification standard since its noise figure and noise parameters can be directly computed from the device S-parameters. The common-gate cold-FET transistor behaves as a variable attenuator in function of the bias point, and their noise parameters are the same order of magnitude as the active device ones. Besides, the common-gate cold-FET transistor can also be used to check the accuracy of the noise figure setup [11]. However, the common-gate cold-FET configuration is not a common on-wafer FET configuration and its implementation requires additional technological steps. For example, a specific bonding to become the transistor in common-gate configuration or a specific foundry design, are needed. For on-wafer transistors, the common-source is the most common configuration, and therefore the implementation of the common-source cold-FET configuration is straightforward. Even though the common-source cold-FET exhibits a large noise figure (around 10 dB) [11], it can be used as noise verification standard, but not to check the accuracy of the noise figure setup (especially, when noise figure values less than 2 dB have to be measured). For these reasons, in this work a common-source cold-FET with gate forward biased is proposed to validate the noise figure measurements and the noise parameters of on-wafer transistors only. Like the common-gate cold-FET, the common-source cold-FET exhibits mismatches close to an active device, therefore the noise figure measurements are performed in a similar condition. Furthermore, the performance of both the tuner method and the F_{50} method for determining the noise parameters in the frequency range of 5-10 GHz are validated using the common-source cold-FET as verification standard.

It is important to comment that the common-source cold-FET configuration under reverse bias has been used as noise source [13-14]; but not as calibration element due to large

noise level. By contrast, the common-source cold-FET under the forward bias behaves as attenuator it can be used to verify noise figure measurements.

2. Noise figure and noise parameters of the common-source cold-FET

A common-source cold-FET configuration is proposed to validate the measured noise figure and the noise parameters extracted by the F_{50} and tuner methods. The common-source cold-FET is implemented by using a common-source MESFET biased with $V_{GS} > V_{bi} > 0$ (V_{bi} is the "built-in voltage") and floating V_{DS} (open drain). The procedure to obtain the noise parameters is described next.

2.1. Computation of the passive device noise parameters using S-parameters

Since the common-source cold-FET is a passive element, its noise figure is given by [15]:

$$F = L, \tag{1}$$

where L are the device losses computed from the S-parameters. The available gain is $G = 1/L$.

On the other hand, the common-source cold-FET's noise parameters can also be computed from the S-parameters through the correlation matrices, as described as follows. For passive devices, the correlation matrix, in its chain representation $\mathbf{C^{AT}}$, is determined from [16,17] as

$$\mathbf{C^{AT}} = 2kT_a\Delta f \mathbf{P^{ZA}} \left\{ \mathbf{Z^D} + \mathbf{Z^{D^\dagger}} \right\} \mathbf{P^{ZA^\dagger}}, \tag{2}$$

Where k denotes the Boltzmann's constant (1.3807×10^{-23} JK^{-1}), T_0 is the standard temperature (290 K) and Δf is the incremental noise bandwidth. The superscript '†' denotes the conjugate transpose, T_a is the room temperature (300 K), $\mathbf{Z^D}$ is the device impedance matrix computed from its S-parameter measurements. Finally, $\mathbf{P^{ZA}}$ is the transformation matrix from impedance to chain representation [17], given by

$$\mathbf{P^{ZA}} = \begin{bmatrix} 1 & \frac{Z_{11}^D}{Z_{21}^D} \\ 0 & \frac{1}{Z_{21}^D} \end{bmatrix}. \tag{3}$$

The noise parameters can be derived from $\mathbf{C^{AT}}$ [12,17], since

$$\mathbf{C^{AT}} = \begin{bmatrix} C_{11}^{AT} & C_{12}^{AT} \\ C_{21}^{AT} & C_{22}^{AT} \end{bmatrix} = 4kT_0\Delta f \begin{bmatrix} R_n & \frac{1}{2}\left(F_{\min}-1\right) - R_n Y_{\text{opt}}^* \\ \frac{1}{2}\left(F_{\min}-1\right) - R_n Y_{\text{opt}} & R_n \left|Y_{\text{opt}}\right|^2 \end{bmatrix}. \tag{4}$$

Then, from Eq. (4), the noise parameters are given as

$$R_n = \frac{C_{11}^{AT}}{4kT_0\Delta f}, \tag{5}$$

$$G_{\text{opt}} = \sqrt{\frac{C_{22}^{AT}}{C_{11}^{AT}} - \left(\frac{Im\left(C_{12}^{AT}\right)}{C_{11}^{AT}}\right)^2}, \tag{6}$$

$$B_{\text{opt}} = \frac{Im\left(C_{12}^{AT}\right)}{C_{11}^{AT}}, \tag{7}$$

and

$$F_{\min} = 1 + \frac{1}{2kT_0\Delta f}\left[C_{12}^{AT} + C_{11}^{AT} Y_{\text{opt}}^*\right]. \tag{8}$$

The asterisk denotes the complex conjugate.

2.2. Determination of the noise parameters using the F_{50} technique

In the F_{50} technique the noise parameters are determined from the knowledge of the device noise model and from the measurements of its noise figure, at different frequencies, when a source admittance is connected to the input of the DUT [9-10]. The analysis of the noise equivalent circuit allows us to determine the correlation matrix, $\mathbf{C^{AT}}$ [10,16], which models the whole noise transistor behavior. Then, from the knowledge of $\mathbf{C^{AT}}$ the noise parameters are computed according to the procedure described next. It is important to comment that, to the author's knowledge, noise analysis of the common-source cold-FET applying the F_{50} technique has not been reported yet.

The active region of the transistor, biased as a cold-FET, is modeled as a Schottky diode in series with a channel resistance, whose impedance is denoted as $\mathbf{Z}^{\text{int}}$, shown in Fig. 1(a). The small-signal equivalent circuit of the common-source cold-FET is shown in Fig. 1(b) [18], where the noise sources are also included. The parasitic elements (R_g, R_d, R_s, L_g, L_d, L_s) are bias independent, while the active region modeled by $\mathbf{Z}^{\text{int}}$ is bias dependent. The parasitic elements of the equivalent circuit are extracted according to the method described by Reynoso *et al*. [18]. Once the parasitic elements are known, then $\mathbf{Z}^{\text{int}}$ is de-embedded.

The noise sources of the intrinsic transistor are represented as noise source voltages e_{gs} and e_{ds}, where the former is associated to the gate-source terminal and the later is associated to the drain-source terminal. The intrinsic noise sources e_{gs} and e_{ds} are arranged into the correlation matrix

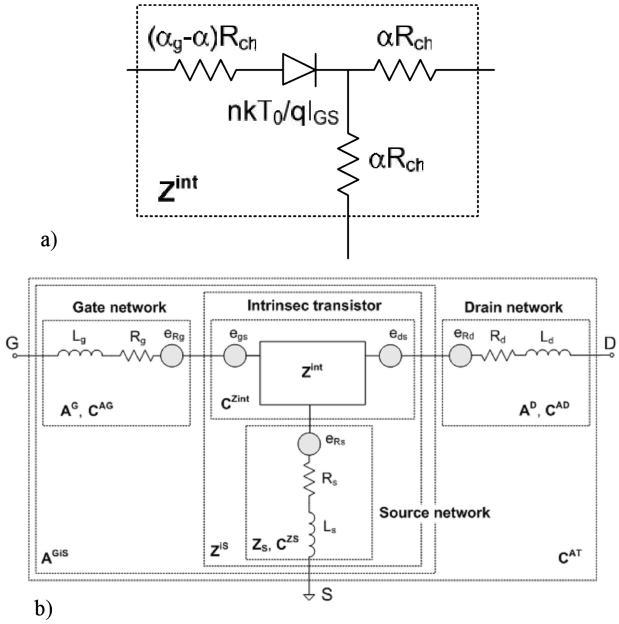

FIGURE 1. Common-source cold-FET: (a) Equivalent circuit for the intrinsic transistor. Note: α_g and α are the factors related to the gate-source current distribution, and to the gate-drain current distribution, respectively. At low current values, α_g =1/3 and α =1/2. R_{ch} is the channel resistance, n is the ideality factor and q is the electron charge. (b) Total electrical equivalent circuit, divided in networks and including noise sources.

denoted as $\mathbf{C^{Zint}}$. The noise contribution of the parasitic elements is modeled by means of the noise source voltages e_{Rg}, e_{Rd} and e_{Rs}, associated to the gate, the drain and the source parasitic resistances, respectively.

To obtain the total correlation matrix, the equivalent circuit is divided into four networks, as shows in Fig. 1(b).

To model the noise contribution of the intrinsic transistor, the impedance matrix representation $\mathbf{C^{Zint}}$ is given by:

$$\mathbf{C^{Zint}} = \begin{bmatrix} \overline{e_{gs}^2} & \overline{e_{gs}e_{ds}^*} \\ \overline{e_{gs}e_{gs}^*} & \overline{e_{ds}^2} \end{bmatrix} = \begin{bmatrix} C_{11}^{\text{int}} & C_{12}^{\text{int}} \\ C_{21}^{\text{int}} & C_{22}^{\text{int}} \end{bmatrix}. \quad (9)$$

Next, the correlation matrix associated to the source network, $\mathbf{C^{ZS}}$, is added to $\mathbf{C^{Zint}}$:

$$\mathbf{C^{ZiS}} = \mathbf{C^{Zint}} + \mathbf{C^{ZS}}, \quad (10)$$

where $\mathbf{C^{ZS}} = 2kT_0\Delta f\left(\mathbf{Z_S} + \mathbf{Z_S^{\dagger}}\right)$, $\mathbf{Z}_S$ being the impedance matrix of the source network. Then, the matrix $\mathbf{C^{ZiS}}$ is transformed to the chain representation and the gate and drain noise contribution represented by the $\mathbf{C^{AG}}$ and $\mathbf{C^{AD}}$ correlations matrix are added. Therefore, the correlation matrix $\mathbf{C^{AT}}$ is defined as

$$\begin{aligned}\mathbf{C^{AT}} = {} & \mathbf{A^{GiS}C^{AD}}\left(\mathbf{A^{GiS}}\right)^{\dagger} \\ & + \mathbf{A^{G}P^{ZAiS}C^{Zint}}\left(\mathbf{A^{G}P^{ZAiS}}\right)^{\dagger} \\ & + \mathbf{A^{G}P^{ZAiS}C^{ZS}}\left(\mathbf{A^{G}P^{ZAiS}}\right)^{\dagger} + \mathbf{C^{AG}}, \end{aligned} \quad (11)$$

where $\mathbf{A^G}$ is the ABCD matrix of the gate network, $\mathbf{A^{GiS}}$ is the ABCD matrix of the gate- intrinsic-source networks and $\mathbf{P^{ZAiS}}$ is the transformation matrix from the impedance to chain representation of the intrinsic-source networks [17]. This matrix is given by

$$\mathbf{P^{ZAiS}} = \begin{bmatrix} 1 & \frac{Z_{11}^{iS}}{Z_{21}^{iS}} \\ 0 & \frac{1}{Z_{21}^{iS}} \end{bmatrix}, \quad (12)$$

where $\mathbf{Z^{iS}}$ is the impedance matrix of the intrinsic transistor in series with the source network. Equation (11) can be expressed as

$$\mathbf{C^{AT}} = \mathbf{C^{AEXT}} + \mathbf{C^{AINT}}, \quad (13)$$

with

$$\begin{aligned}\mathbf{C^{AEXT}} = {} & \mathbf{A^{GiS}C^{AD}}\left(\mathbf{A^{GiS}}\right)^{\dagger} \\ & + \mathbf{A^{G}P^{ZAiS}C^{ZS}}\left(\mathbf{A^{G}P^{ZAiS}}\right)^{\dagger} + \mathbf{C^{AG}} \end{aligned} \quad (14)$$

and

$$\mathbf{C^{AINT}} = \mathbf{A^{G}P^{ZAiS}C^{Zint}}\left(\mathbf{A^{G}P^{ZAiS}}\right)^{\dagger}. \quad (15)$$

The extrinsic noise correlation matrix, $\mathbf{C^{AEXT}}$, includes the whole effect of thermal noise associated to the extrinsic elements, and this contribution can be determined as long as their values are known. The intrinsic correlation matrix, $\mathbf{C^{AINT}}$, represents noise generated in the intrinsic transistor. The contribution of the Schottky diode shot noise can also be included by adding a current source noise (i_{shot}) in parallel to the diode. The spectral density, $\overline{i_{\text{shot}}}^2$, can be determined from low frequency noise measurement, and is considered as an extrinsic noise source [10]. According to the procedure described before (from Eq. (9) to (11)), the total shot noise correlation matrix is given by:

$$\mathbf{C}_{shot} = \mathbf{A^{G}P^{ZAiS}}\begin{bmatrix} \overline{e_{\text{shot}}^2} & 0 \\ 0 & 0 \end{bmatrix}\left(\mathbf{A^{G}P^{ZAiS}}\right)^{\dagger}. \quad (16)$$

Where

$$\overline{e_{\text{shot}}^2} = |Z_{\text{did}}|^2\,\overline{i_{\text{shot}}^2},$$

Z_{did} is the diode impedance ($Z_{\text{did}} = \frac{nkT_0}{qI_{\text{GS}}}$), and $\overline{i_{\text{shot}}}^2 = 2qI_{\text{GS}}$. Then, if the shot noise is included in the equivalent circuit, the shot noise correction matrix, $\mathbf{C}_{\text{shot}}$, should be added to the Eq. (14). In the same way, the Eq. (2) defines only the cold-FET thermal noise contribution (considering as passive device); if the shot noise is considered, $\mathbf{C}_{\text{shot}}$ is added to Eq. (2). The shot noise contribution in the noise figure will be discussed at the results section.

It is important to comment that the cold-FET configuration can be represented by two Schottky diodes: one due to the gate-source contacts and the other one due to the gate-drain contacts. Then, the $\mathbf{C}_{\text{shot}}$ should be redefined considering the two shot current sources noise, one associated to the

gate-source Schottky diode ($\overline{i^2_{\text{shot\_GS}}}$) and the other one associated to the gate-drain Schottky diode ($\overline{i^2_{\text{shot\_GD}}}$) [14]:

$$\mathbf{C}_{\text{shot}} = \mathbf{A^G P^{ZAiS} Z_{int} H_0} \times \begin{bmatrix} \overline{i^2_{\text{shot\_GS}}} & 0 \\ 0 & \overline{i^2_{\text{shot\_GD}}} \end{bmatrix} \left(\mathbf{A^G P^{ZAiS} Z_{int} H_0}\right)^{\dagger} . \quad (17)$$

Where $\overline{i_{\text{shot\_GS}}}^2 = 2qI_{\text{GS}}$ and $\overline{i_{\text{shot\_GD}}}^2 = 2qI_{GD}$, $\mathbf{H_0}$ is the conversion matrix from an $\overline{\text{ishot\_GS}}^2 - \overline{\text{ishot\_GD}}^2$ noise-source configuration to an admittance noise-source configuration [14], and $\mathbf{Z}_{\text{int}}$ is the impedance of the intrinsic device. However, since in this work the floating drain-source configuration is considered, $I_{\text{GD}} = 0$ and the Eq. (17) is reduced to (16).

As mentioned early, since the common-source cold-FET is a passive device,$\mathbf{C^{Zint}}$, and therefore $\mathbf{C^{AINT}}$, can be determined from the knowledge of $\mathbf{Z^{int}}$. Moreover, to validate the F_{50}technique we assumed that the elements of $\mathbf{C^{Zint}}$ are unknown, and they can be computed from the noise figure by using [16]:

$$F = 1 + \frac{1}{4kT_0 Re\left(Z_g\right)\Delta f} \cdot [1 \;\; Z_g] \cdot \mathbf{C^{AT}} \cdot \begin{bmatrix} 1 \\ Z_g^* \end{bmatrix}, \quad (18)$$

where Z_g is the impedance value of the load presented at the input of the DUT. The noise figure is measured for N_f frequency points. Substituting Eqs. (13) and (15) into Eq. (18), it follow

$$\Delta_i = [1 \;\; Z_{g\,i}] \cdot \mathbf{P} \cdot \mathbf{C^{Zint}} \cdot \mathbf{P}^{\dagger} \cdot \begin{bmatrix} 1 \\ Z_{g\,i}^* \end{bmatrix}, \quad (19)$$

with i=1,.., N_f, and

$$\Delta_i = 4kT_0 Re(Z_{g\,i})\Delta f[F_i - 1] - [1 \; Z_{g\,i}] \cdot \mathbf{C^{AEXT}} \cdot \begin{bmatrix} 1 \\ Z_{g\,i}^* \end{bmatrix}, \quad (20)$$

and

$$\mathbf{P} = \mathbf{A^G P^{ZAiS}}. \quad (21)$$

Since the $\mathbf{C^{Zint}}$ is an Hermitian matrix, Im(C^{int}_{11}) = Im(C^{int}_{22}) = 0, $C^{\text{int}}_{21} = (C^{\text{int}}_{12})^*$ and $C^{\text{int}}_{12} = \text{Re}(C^{\text{int}}_{12}) + j\text{Im}\left(C^{\text{int}}_{12}\right)$, Eq. (19) becomes

$$\Delta_i = [M_{i1} \;\; M_{i2} \;\; M_{i3} \;\; M_{i4}] \begin{bmatrix} C^{\text{int}}_{11} \\ C^{\text{int}}_{22} \\ \text{Re}(C^{\text{int}}_{12}) \\ \text{Im}(C^{\text{int}}_{12}) \end{bmatrix}, \quad (22)$$

where

$$M_{i1} = |P_{11}|^2 + |Z_{g\,i}|^2 |P_{21}|^2 + Z_{g\,i} P_{11}^* P_{21} + Z_{g\,i}^* P_{11} P_{21}^* , \quad (23)$$

$$M_{i2} = |P_{12}|^2 + |Z_{g\,i}|^2 |P_{22}|^2 + Z_{g\,i} P_{12}^* P_{22} + Z_{g\,i}^* P_{12} P_{22}^* , \quad (24)$$

$$M_{i3} = 2\text{Re}(P_{11} P_{12}^*) + 2\,|Z_{g\,i}|^2 \text{Re}(P_{21} P_{22}^*) + 2\text{Re}(Z_{g\,i} P_{12}^* P_{21}) + 2\text{Re}(Z_{g\,i}^* P_{11} P_{22}^*) \quad (25)$$

and

$$M_{i4} = -2\text{Im}(P_{11} P_{12}^*) - 2\,|Z_{g\,i}|^2 \text{Im}(P_{21} P_{22}^*) - 2\text{Im}\left(Z_{g\,i} P_{12}^* P_{21}\right) - 2\text{Im}\left(Z_{g\,i}^* P_{11} P_{22}^*\right). \quad (26)$$

Equation (22) has four unknowns, so at least four frequency points are needed to solve the system. When $N_f > 4$, the system is redundant. On the other hand, the elements of $\mathbf{C^{Zint}}$ can be modeled by a frequency dependent L-order polynomial:

$$C^{\text{int}}_{\text{mn}} = \sum_{l=0}^{L} C^l_{\text{mn}} f_i^l, \quad (27)$$

where $C^{\text{int}}_{\text{mn}}$ refers to C^{int}_{11}, C^{int}_{22}, $Re\left(C^{\text{int}}_{12}\right)$ or Im$\left(C^{\text{int}}_{12}\right)$. When L=1, and substituting (27) into (22), the following matrix equation results:

$$\begin{bmatrix} \Delta_1 \\ \vdots \\ \Delta_i \\ \vdots \\ \Delta_{Nf} \end{bmatrix} = \begin{bmatrix} M_{11} & M_{11} f_1 & M_{12} & M_{12} f_1 & M_{13} & M_{13} f_1 & M_{14} & M_{14} f_1 \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ M_{i1} & M_{i1} f_2 & M_{i2} & M_{i2} f_2 & M_{i3} & M_{i3} f_2 & M_{i4} & M_{i4} f_2 \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ M_{Nf\,1} & M_{Nf\,1} f_{Nf} & M_{Nf\,2} & M_{Nf\,2} f_{Nf} & M_{Nf\,3} & M_{Nf\,3} f_{Nf} & M_{Nf\,4} & M_{Nf\,4} f_{Nf} \end{bmatrix} \begin{bmatrix} C^0_{11} \\ C^1_{11} \\ C^0_{22} \\ C^1_{22} \\ \text{Re}(C_{12})^0 \\ \text{Re}(C_{12})^1 \\ \text{Im}(C_{12})^0 \\ \text{Im}(C_{12})^1 \end{bmatrix} \quad (28)$$

Since Eq. (28) is not a square matrix, an analytical solution does not exist. To solve Eq. (28) a numerical optimization method is then required.

The optimization's goal is to minimize the error function, ε_{F50}, defined as,

$$\varepsilon_{F50} = \frac{1}{N_f}\left(\sum_{i=1}^{Nf}\Big|\,(M_{i1}+M_{i1}f_i)\,C_{11}^{\text{int}} + (M_{i2}+M_{i2}f_i)\,C_{22}^{\text{int}} + (M_{i3}+M_{i3}f_i)\,\text{Re}(C_{12}^{\text{int}}) + (M_{i4}+M_{i4}f_i)\,\text{Im}(C_{12}^{\text{int}}) - \Delta_i\Big|^2\right)^{1/2}, \quad (29)$$

where Δ_i is computed from Eq. (20).

The initial values are obtained as follow: C_{22}^0, $\text{Re}(C_{12})^0$ and $\text{Im}(C_{12})^0$ are computed applying the pseudo-inverse to (28), C_{11}^0 is determined from $C_{11}^0 = 4kT_a\text{Re}(Z_{\text{int}}(1,1))$ [10], and C_{22}^1, $\text{Re}(C_{12})^1$, $\text{Im}(C_{12})^1$ and C_{11}^1 are equal to zero. The optimization order is: C_{22}^0, C_{22}^1, C_{11}^0, C_{11}^1, $\text{Re}(C_{12})^0$, $\text{Re}(C_{12})^1$, $\text{Im}(C_{12})^0$, and $\text{Im}(C_{12})^1$. This order has been established after observing how the variations of $\mathbf{C}^{\mathbf{Z_{int}}}$ elements affect the behavior of the noise parameters. Besides, the following restrictions are taken into account in the optimization process:

$$C_{11}^{\text{int}} \geq 0, \quad C_{22}^{\text{int}} \geq 0,$$
$$0 \leq \left|\rho = \frac{C_{12}^{\text{int}}}{\sqrt{\left|C_{11}^{\text{int}}\right|^2\left|C_{22}^{\text{int}}\right|^2}}\right| \leq 1. \quad (30)$$

Once $\mathbf{C}^{\mathbf{Zint}}$ has been determined, the noise parameters are computed from $\mathbf{C}^{\mathbf{AT}}$ (see Eqs. (13)-(15) and (5)-(8)).

2.3. Determination of noise parameters applying the tuner technique

In order to verify the correct extraction of the noise parameters we compare the results obtained with the proposed method with the results obtained using the tuner technique. Noise parameter extraction based on the tuner system uses the measure of the noise figure under different input admittances (at least seven different admittances). The noise parameters are determined from the solution of the noise figure equation defined as function of the noise parameters and of the source admittance, which is given by [3,4]

$$F\left(Y_{g\,j}\right) = F_{\min} + \frac{R_n}{G_{g\,j}}\left[\left(G_{g\,j}-G_{\text{opt}}\right)^2 + \left(B_{g\,j}-B_{\text{opt}}\right)^2\right], \quad (31)$$

where $Y_{gj} = G_{gj}+B_{gj}$, with j=1, . . . , N_s, and N_s is the number of points of Y_g at which F is measured. Equation (31) can be rewritten, according with the Lane method [4], as:

$$F\left(\Gamma_{g\,j}\right) = A + BG_{g\,j} + \frac{C + B\left(B_{g\,j}\right)^2 + DB_{g\,j}}{G_{g\,j}}, \quad (32)$$

where

$$F_{\min} = A + \sqrt{4BC - D^2}\,, \quad (33)$$

$$R_n = B\,, \quad (34)$$

$$B_{\text{opt}} = -\frac{D}{2B}\,, \quad (35)$$

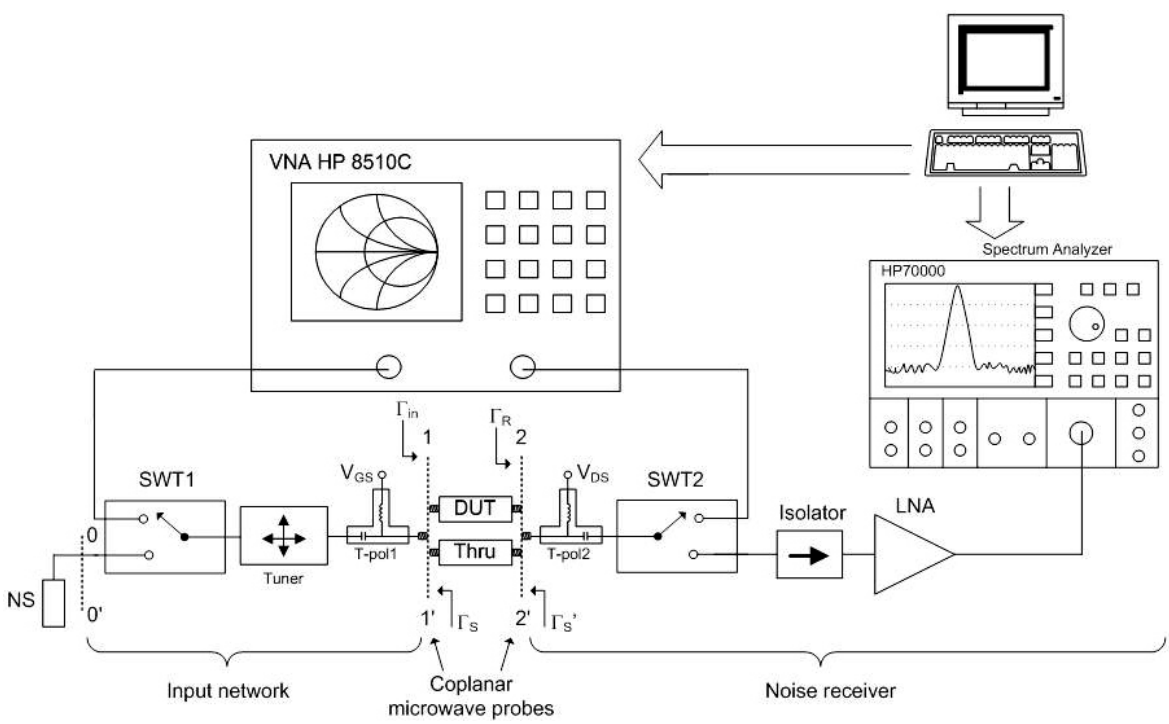

FIGURE 2. Noise figure measurement system.

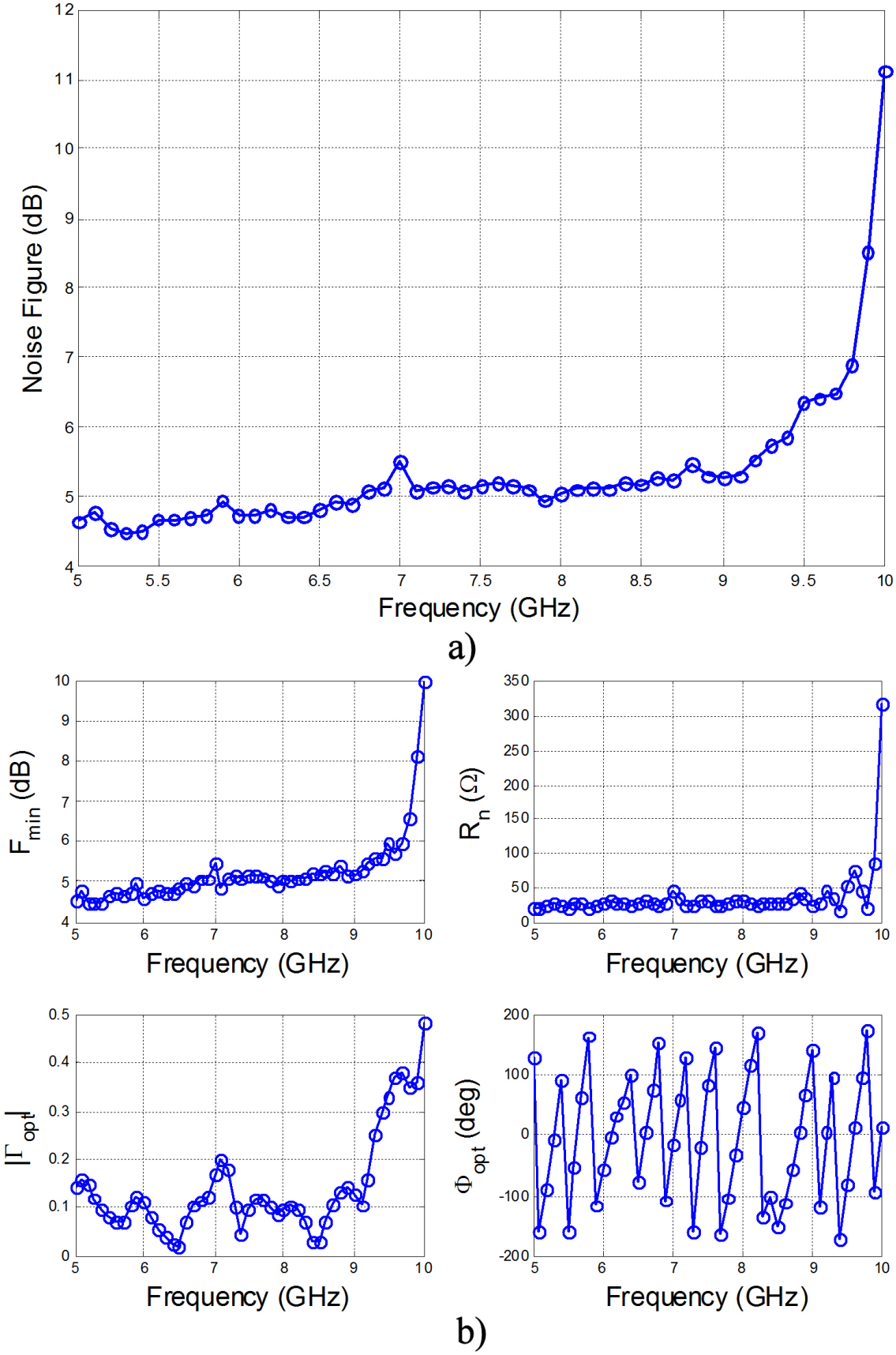

FIGURE 3. a) Noise figure and b) noise parameters of the receiver.

and

$$G_{\text{opt}} = \frac{\sqrt{4BC - D^2}}{2B}. \tag{36}$$

The A, B, C and D parameters can be obtained by applying the least square method.

3. Experimental results

3.1. Noise figure setup

The S-parameters and the noise figure of the device under test have been measured from 5 to 10 GHz using the experimental setup shown in Fig. 2. The setup consists of a vector network analyzer (VNA), a probe station, an input network and a noise receiver. The VNA (HP8510C) is used to measure the S-parameters of the device under test (DUT), and the reflection coefficients of the source, the receiver and the device input (denoted as Γ_S, Γ_R and Γ_{in}, respectively). The on-wafer probe station (SUMMIT-9000 from Cascade-Microtech) is used as a test fixture for inserting the DUT. The input network consists of one switch (SWT1) to select the DUT input connection between the VNA or the tuner input, a tuner (focus iCCMT-5020-TC), the V_{GS} bias-tee, and a coplanar microwave probe for connecting the DUT input. The noise receiver consists of a spectrum analyzer (SA) (HP70000 series), a low-noise amplifier (LNA), one switch (SWT2) to select the output DUT connection between the VNA or the LNA input, an isolator, the V_{DS} bias-tee, and a coplanar microwave probe for connecting the DUT output. All measurements are controlled with an external PC via GPIB and Ethernet. Prior to measure the device noise figure, the system noise must be calibrated according to the procedure described in [19]. While the system noise calibration is performed, a thru is connected at the coplanar planes (1-1'and 2-2') instead of the DUT. A coaxial HP346C noise source (NS), connected at the 0-0'plane, is used to calibrate the noise system. In Fig. 3(a)-(b) the receiver's noise figure and its noise parameters are reported. The noise figure is measured with the NS at cold-state [19]. It is important to mention that the isolator is used to avoid reflection between the DUT and the noise receiver. A possible inconvenient of using an isolator is that the measurement frequency range is fixed by the operation frequency of the isolator. This is the reason why the noise figure measurements shown in Fig. 3(a)-(b) increase at frequencies greater than 9 GHz.

3.2. Common-source cold-FET noise figure and noise parameters

An on-wafer MESFET, featured by a 0.2 μm gate-length and a 2×60 μm gate-width, has been used in our investigation. The MESFET has been biased as common-source cold-FET, with floating drain, and V_{GS} = 0.76 V and I_{GS}=5 mA. According to the results reported by Reynoso *et al.* [18], the floating drain configuration overcomes the inconsistencies between DC and RF techniques to extract the parasitic resistances and the equations involves are an extension of those presented by Dambrine *et al.* [20]. From the measured S-parameters, shown in Fig. 4, it can be seen that the common-source cold-FET is a mismatched device (return loss > 10 dB) with 14 dB of transmission loss.

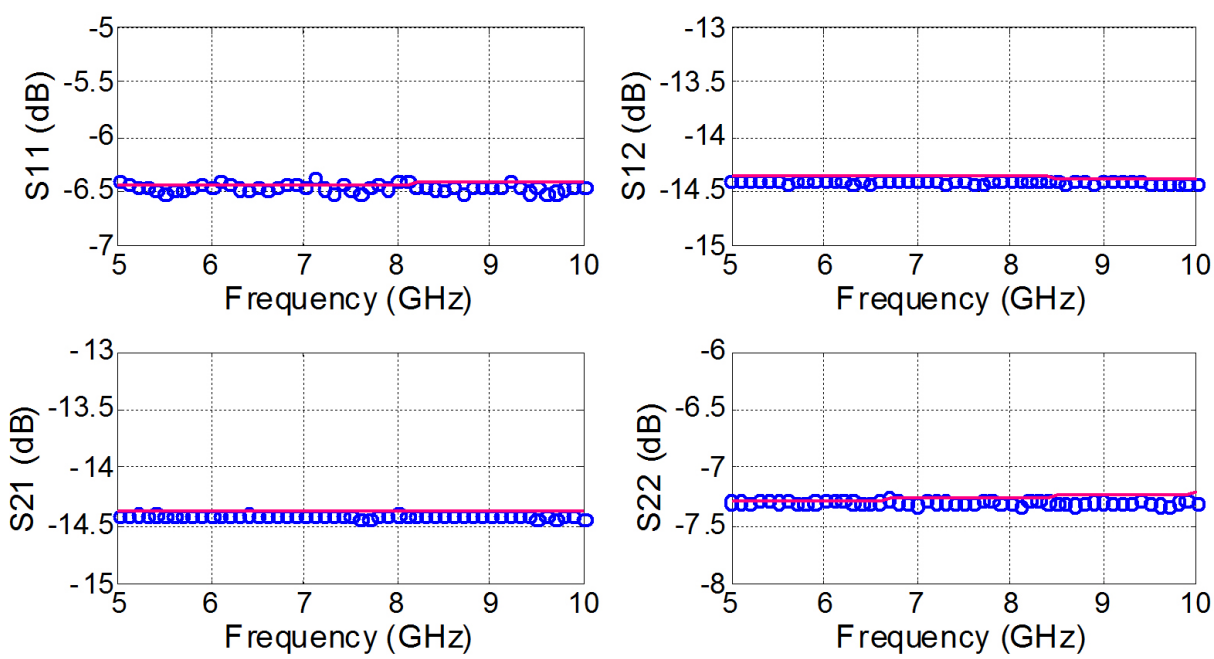

FIGURE 4. S-parameters of the common-source cold-FET biased with V_{GS}=0.76 V and I_{GS}=5 mA, measured (o) and calculated (–) using the equivalent circuit elements.

TABLE I. Equivalent circuit elements of the common-source cold-FET, biased with V_{GS}=0.76V and I_{GS}=5mA

R_g (Ω)	3.47	L_g (pH)	49.05
R_s (Ω)	9.19	L_s (pH)	3.34
R_d (Ω)	11.85	L_d (pH)	76.46
Ideality factor (n)		1.28	

The elements value of the equivalent circuit, are extracted according to the method described by Reynoso *et al.* [18], are given in Table I. In Fig. 4 the S-parameters measured and calculated using the equivalent circuit are compared and good correlation is observed.

Theoretical values of the common-source cold-FET noise figure have been computed by applying Eq. (1). The noise parameters have been extracted with both the F_{50} and the tuner techniques. To apply the tuner method, different admittance values (N_s >7) have been used to reduce the measurements errors [4-8].

To verify the noise figure measurements, the experimental common-source cold-FET noise figure is compared with the noise figure predicted by Eq. (1), and the comparison is reported in Fig. 5. The noise figure has been measured under matched input admittance (≈50Ω) condition. The theoretical noise figure shows a small ripple which is produced by mismatches of the DUT input. At frequencies lower than 8 GHz, the measured noise figure shows a good agreement with the theoretical results. Due to the isolator performance, at higher frequencies the experimental noise figure exhibits a ripple whose value oscillates around ± 1 dB. This ripple fixes the accuracy of the measurements.

In order to investigate the shot noise contribution in the noise figure of the common-source cold-FET, $\mathbf{C^{AT}}$ is calculated including the shot noise contribution as follow:

$$\mathbf{C^{AT}} = 2kT_a\Delta f\mathbf{P^{ZA}}\left\{\mathbf{Z^{D}} + \mathbf{Z^{D}}^{\dagger}\right\}\mathbf{P^{ZA}}^{\dagger} + \mathbf{A^{G}P^{ZAiS}}\begin{bmatrix} \overline{e^2_{\text{shot}}} & 0 \\ 0 & 0 \end{bmatrix}\left(\mathbf{A^{G}P^{ZAiS}}\right)^{\dagger}. \quad (37)$$

The results of the noise figure calculated with (18) by using (2) and (37), respectively, are reported in Fig. 5. The noise figure calculated including the contribution of shot noise is identical to the noise figure calculated considering only the thermal contribution. Both results agree with the noise figure calculated by using S-parameters.

The F_{50} method was applied considering only the thermal noise contribution, since the shot noise does not have a significant effect on the noise figure. In Fig. 6 are reported the values of the intrinsic correlation matrix ($\mathbf{C^{Zint}}$) computed by using the F_{50} method and they are compared to experimental data calculated from $\mathbf{Z^{int}}$ $\left(\mathbf{C^{Zint}} = 2kT_a\Delta f\left\{\mathbf{Z^{int}} + \mathbf{Z^{int}}^{\dagger}\right\}\right)$. It is important to comment that $\mathbf{Z^{int}}$ is determined after performing a de-embedding of the parasitic elements to the impedance matrix,

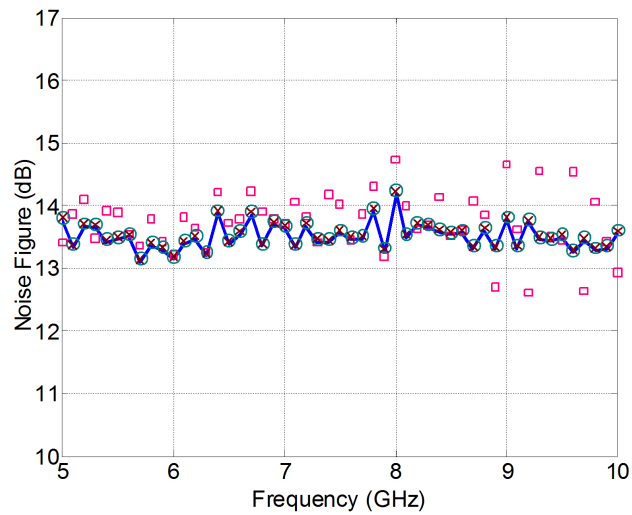

FIGURE 5. Noise figure of a common-source cold-FET (biased with V_{GS}=0.76 V and I_{GS}=5 mA): measured (□), calculated by using S parameters (Eq. (1)) (–), and calculated by using $\mathbf{C^{AT}}$ without shot noise (Eq. (2)) (x), and with shot noise (Eq. (37)) (o).

$\mathbf{Z}^D$ (obtained from measurements of S-parameters). Notice that the values of $\mathbf{C^{Zint}}$ determined from F_{50} method predict the experimental data of $\mathbf{C^{Zint}}$ calculated by using the measured S-parameters.

Noise parameters determined with the F_{50}, the tuner technique and the computed from the correlation matrix $\mathbf{C^{AT}}$ (Eqs. (2)-(8)) are reported in Fig. 7. It is observed that the noise parameters computed by F_{50} are similar to those predicted by the S-parameters. On the other hand, the noise parameters extracted with the tuner technique show a ripple. The ripple in $F_{\min}$ is ±0.5 dB at frequencies lower than 9 GHz and the ripple becomes larger as the frequency increases. The ripple in R_n is ±13Ω at frequencies lower than 8 GHz, and increases at higher frequencies. The ripple in the phase of the optimum reflection coefficient is ±3 degrees. It is important to mention that the mean values of the noise parameters extracted with the tuner method are in good agreement with both the calculated value using S-parameters and the computed value using F_{50}. According to the results, we can conclude that the tuner technique is more sensible to measurement errors than the F_{50} technique.

Noise figure has also been determined from the noise parameters extracted with both the F_{50} technique and the tuner technique. The results are plotted in Fig. 8. Furthermore, a comparison of the noise figure computed from the S parameters (Eq. (1)) with those determined from the noise parameters is also reported in Fig. 8. It should be noticed that the noise figure determined with the tuner and the F_{50} methods agree quite well with the noise figure computed from the S-parameters up to 8 GHz. At higher frequencies the tuner results show a significant ripple, which is associated to the experimental noise figure, as mentioned before.

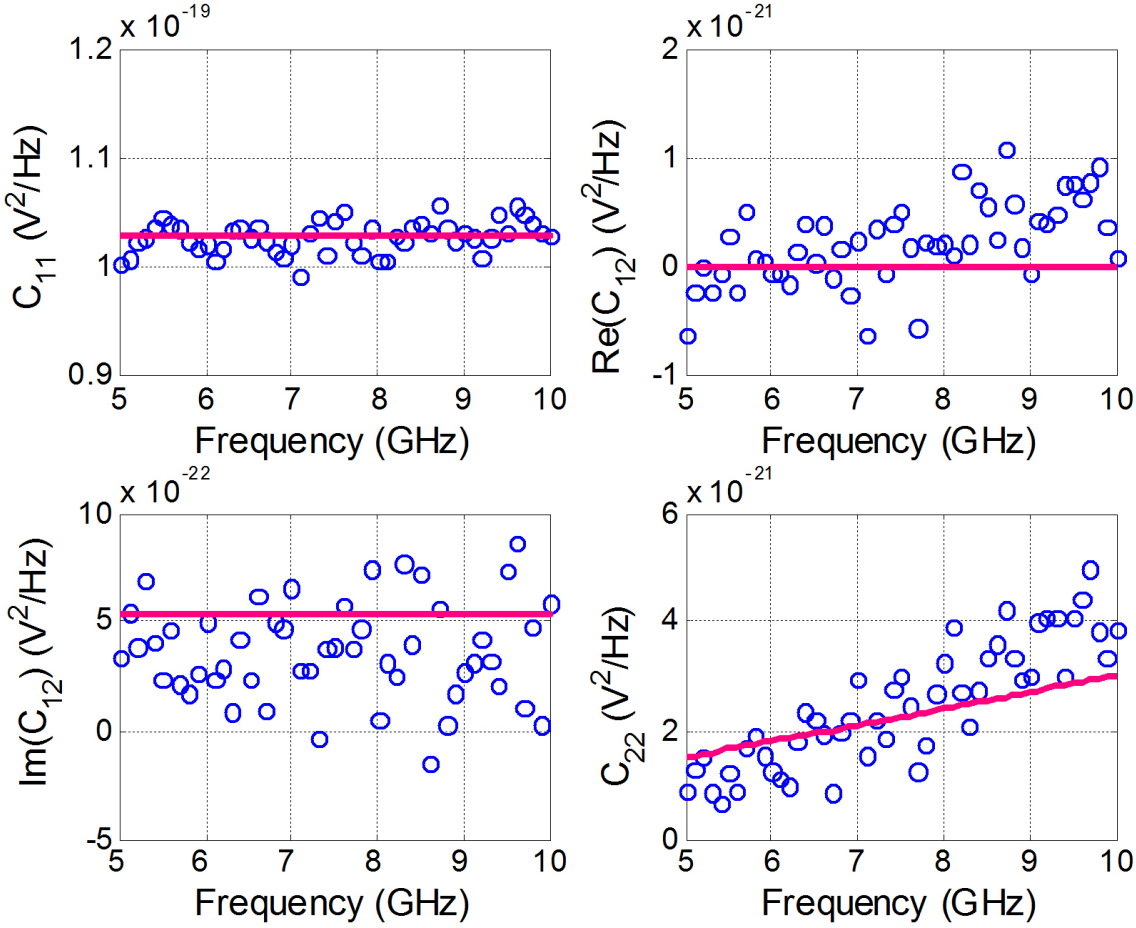

FIGURE 6. Elements of the intrinsic correlation matrix: (–) computed from F_{50} and by using (o) the S-parameters.

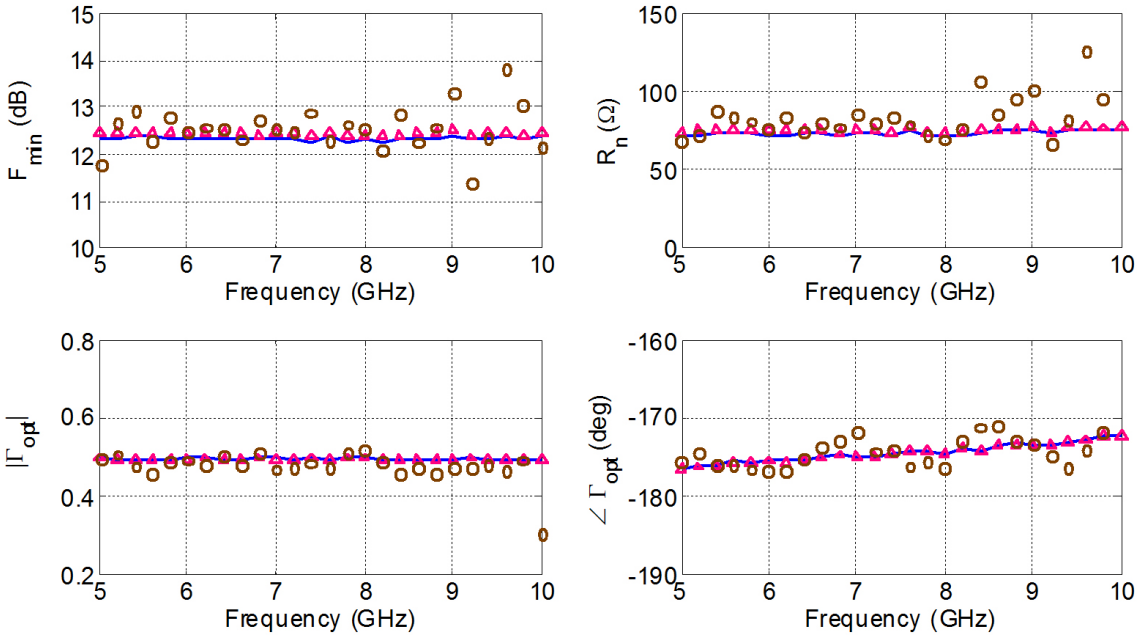

FIGURE 7. Common-source cold-FET's noise parameters: theoretical (computed from the S parameters (–)) and extracted with the F_{50} (Δ), and tuner (o) techniques. The cold-FET has been biased with V_{GS}=0.76 V and I_{GS}=5 mA.

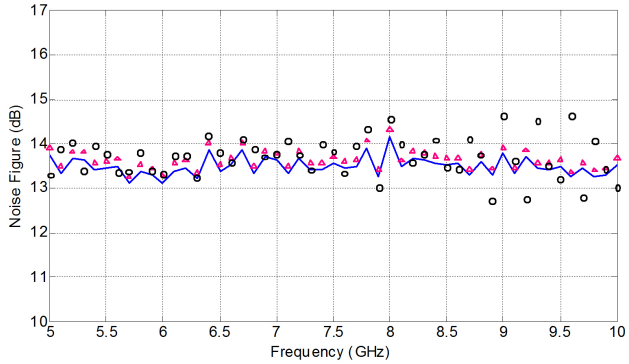

FIGURE 8. Noise figure of the common-source cold-FET (biased with V_{GS}=0.76 V and I_{GS}=5 mA): computed from the S parameters (Eq. (1)) (–), and by applying the results of the noise parameters determined with the F_{50} (Δ) and the tuner (o) techniques.

4. Conclusions

The S-parameters of a common-source cold-FET have been used to validate the noise figure measurements and the extraction of noise parameters of on-wafer devices. Since the common-source cold-FET behaves as a passive device, its noise figure and noise parameters can be directly computed from its S-parameters. The experimental noise parameters have been extracted using the tuner and F_{50} methods. A good correlation between the measured and calculated noise figure of the common-source cold-FET is observed. Similarly, the experimental noise parameters agree with the noise parameters computed with the S-parameters. Furthermore, the shot noise contribution on the common-source cold-FET noise figure has been investigated. Our results indicate that the shot noise contribution is not significant. Finally, these results demonstrate that the common-source cold-FET can be used to validate the noise figure measurements and on-wafer transistor noise parameters extraction.

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