A simple de-embeding method for on-wafer RF CMOS FET using two microstrip lines

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This letter deals with the de-embedding of on-wafer CMOS FETs embedded in symmetrical and reciprocals pads. A de-embedding method, that uses a calibrated vector network analyzer and two microstrip lines fabricated on a lossy SiO_2-Si substrate, is introduced. The proposed method not only allows the characterization on the interconnection lines but also allows the characterization of the CMOS pads. Our results demonstrate that a shunt admittance does not suffice to properly model CMOS pads. Experimental S-parameters data of on-wafer CMOS FETs de-embedded with the proposed L-L method, Mangan and the Pad-Open-Short De-embedded (PSOD) methods are compared. The S-parameter data, de-embedded with the PSOD and the proposed two-tier L-L show high correlation, validating the proposed de-embedding method.

Keywords: Electrical measurement; microwave circuits; field effect devices; high speed techniques.

En este trabajo se presenta un método para desincrustar transistores CMOS de efecto de campo embebidos en *pads* simétricos y recíprocos. El método de desincrustación propuesto utiliza como estándares de calibración dos líneas de microcinta, fabricadas sobre un substrato de Si con pérdidas. El método propuesto no solo permite la caracterización de las líneas de interconexión sino también de los *pads* CMOS. Los resultados experimentales demuestran que una simple admitancia no es la manera apropiada para modelar los *pads* CMOS. Se comparan datos experimentales de parámetros S de transistores de efecto de campo CMOS en oblea desincrustados con el método propuesto L-L, el de Mangan y el Pad-Open-Short De-embededded (PSOD). Los datos de los parámetros S desincrustados con los métodos PSOD y el propuesto muestran una alta correlación, validando el método de desincrustación que se reporta en este trabajo.

Descriptores: Mediciones eléctricas; circuitos de microondas; dispositivos de efecto de campo; técnica de alta velocidad.

PACS: 84.37.+q; 84.40.Dc; 85.30Tv; 06.60.Jn

1. Introduction

When CMOS FETs are embedded in lines and pads, a de-embedding method is required in order to determine the CMOS FET S-parameters. Several and different methods have been proposed to de-embed the on-wafer CMOS FET S-parameters [1-7]. These methods represent the pads and interconnection lines as admittances and impedances, respectively, and use dummies structures (pad, open, short, etc.) measurements for de-embedding the CMOS FET S-parameters. An important drawback is that open or short conditions in the dummy structures are difficult to achieve in a broadband frequency range. Moreover, in the calibration process of the VNA, identical calibration structures (pad, open, short) in ports one and two are required, otherwise the de-embedded S-parameters procedure is incorrect. Therefore a simplest but accurately de-embedding method is sought.

A common procedure to determine the S-parameters of the on-wafer CMOS FET is by characterizing the CMOS pads and the interconnection lines using the two-lines method [8] instead of dummy structures [9]. In that sense, a de-embedding technique reported in Refs. 10 to 11 uses two uniform transmission lines to characterize coaxial connectors. However the theory requires that the connectors have to be symmetrical and reciprocal and these hypotheses are not completely fulfilled in the coaxial connector case. Nevertheless, for on-wafer devices as those shown in Fig.1, these conditions can easily be fulfilled. Thus the purpose in this work is twofold. Demonstrate the advantage of the two lines method [10-12] to de-embed on-wafer CMOS FET embedded in both pads and lines, and to present a new procedure to model accurately the CMOS pads by means of an electrical equivalent circuit (EEC). The knowledge of a CMOS pad electrical equivalent circuit is crucial in the design of RFIC, nonetheless this information is not available in the design rules in spite of being of great help to develop better designs.

Regarding to modeling of the CMOS pads with ground-shielding, [8] and [13] suggested the utilization of a simple shunt admittance to represent the electrical behavior of pads. The shunt admittance is usually represented by a shunt capacitance. Moreover in Ref. 14 the authors suggest adding a series resistance to the shunt capacitance model for improving its frequency response. In Ref. 9, on the other hand, series inductances are added to form a T-network to model the CMOS pads. These inductances allow modeling the discontinuity of

the probe to the pad and from the pad to the interconnection line. Even though the electrical equivalent circuit (EEC) of the pad proposed in Ref. 9 seems to be quite good, the drawback is the lack of a reliable procedure to determine the values of these inductors since they are determined using a trial and error procedure. To overcome this problem, the proposed method, which is based on [10-12], uses an analytical method to obtain the EEC of the CMOS pads. The method assumes that the pads are symmetrical and reciprocal, and by using ABCD matrices, it is possible to compute the elements of the EEC.

To verify whether a simple shunt admittance should be used as an EEC of the CMOS pad, de-embedded S-parameter data of an on-wafer CMOS FET computed with [8] and [12] were used to reproduce the original measurement of the CMOS FET from 0.4 to 20 GHz. Our results demonstrate that a shunt admittance does not suffice to accurately represent the frequency response of CMOS pads. Moreover, due that the proposed CMOS pad-model predicts the measurement data accurately, it is very useful to de-embed the S-parameters of CMOS FET embedded in both pads and interconnection lines.

2. De-embedded Procedure

Figure 1 shows the structure of the CMOS FET used in this work. The transistor is embedded in pads and lossy interconnections lines with a physical length of 54 μm. The pads consist of two metallization layers (M2 and M3) and the ground paths are tied to a single node by a N-WELL layer allowing an isolation of the signal to the substrate.

When the electrical length of the line is small compared to the signal wavelength, one can assume that the interconnection line can be modeled as a lumped circuit. Thus at first sight the simplest solution is to consider the pad and the interconnection line as a lumped passive sub-circuit. Nevertheless, making this assumption leads to an extraction problem of the lumped elements that properly model the effects of the interconnection line, since it is expected a phase difference between the input and the output. De-embeding the S-parameters of the CMOS FET embedded in pads and interconnection lines under the condition mentioned above, will require to use calibration techniques that employ reflect standards (OPEN or SHORT) as TRL. This gives rise to the problem of guaranteeing an OPEN or SHORT condition in all the frequency range of interest, since this condition is very difficult to achieve over a broadband range. Moreover, de-embedding techniques that use dummy structures [1-5] have the same problem with OPEN or SHORT condition over broadband frequency ranges. Modeling the interconnection as a transmission line overcomes such problems.

Transmission lines can be fabricated on SiO_2-Si substrate as explained in Refs. 14 to 16, due to the characteristics of this substrate and the geometry of the interconnection (ε_r, height of the substrate and line width) higher-order modes appear at very high frequencies. It is worth to comment that these higher-order modes are function of the frequency and the transversal dimensions of the interconnection but not of the line length as explained in Ref. 16.

The ABCD matrix of any DUT embedded in a structure as shown in Fig. 1, according to [10-11] is given by:

$$[M_{dut}] = [M_L]^{-1}[M_{LP}]^{-1}[M][M_{RP}]^{-1}[M_L]^{-1}\,, \qquad (1)$$

where $[M]$ represents measured data; $[M_{LP}]$ and $[M_{RP}]$ represent the left and right pad, respectively, and the line used to interconnect the pads with the transistor is referred to as $[M_L]$.

On one hand, when the pads are assumed identical, symmetrical, and reciprocal, its ABCD matrix can be written as:

$$[M_{LP}] = [M_{RP}] = [M_{pad}]\begin{bmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{bmatrix}. \qquad (2)$$

where a_{11}, a_{12}, and a_{21} are the elements of the matrix $[M_{Pad}]$ to be determined. On the other hand, the ABCD matrix of the interconnection lines can be written as:

$$[M_L] = \begin{bmatrix} \cos h(\gamma L) & Z_0 \sin h(\gamma L) \\ \frac{1}{Z_0}\sin h(\gamma L) & \cos h(\gamma L) \end{bmatrix}. \qquad (3)$$

where L, Z_0 and γ are the length, the characteristic impedance, and the propagation constant of the line, respectively. Notice that $[M_{DUT}]$ can be determined as long as $[M_{Pad}]$ and $[M_L]$ are known. When the interconnection lines are nonreflecting, the most common method for determining $[M_{pad}]$ is using the TRL calibration technique, which uses three calibration standards. Moreover, when one is trying to characterize CMOS FETs embedded in pads and interconnection lines of arbitrary characteristic impedance, as that shown in Fig.1, only two calibration elements are required to determine $[M_{pad}]$ and $[M_L]$ [10-11].

Hence, according to the procedure reported in Ref. 10 to 11, a_{11}, a_{12}, a_{21}, Z_0 and γ are determined by means of the ABCD matrix of the two microstrip lines fabricated on Si substrate. Thus, with the help of matrices algebra, it can be obtained the following relations:

$$\begin{pmatrix} n_{11} & n_{12} \\ n_{21} & n_{22} \end{pmatrix}\begin{pmatrix} a_{11} & a_{12} \\ a_{21} & a_{11} \end{pmatrix}^{-1} = \begin{pmatrix} a_{11} & a_{12} \\ a_{21} & a_{11} \end{pmatrix}\begin{pmatrix} \cos h(\gamma L_1) & Z_0 \sin h(\gamma L_1) \\ \frac{1}{Z_0}\sin h(\gamma L_1) & \cos h(\gamma L_1) \end{pmatrix}, \qquad (4)$$

$$\begin{pmatrix} n_{11}-\cos h(\gamma L_1) & \underline{n_{12}} \\ \underline{n_{21}} & n_{11}-\cos h(\gamma L_1) \end{pmatrix}$$

$$= \begin{pmatrix} (n_{12})\frac{a_{21}}{a_{11}} + \left(\frac{1}{Z_0}\sin h(\gamma L_1)\right)\frac{a_{12}}{a_{11}} & \underline{(n_{11}+cosh(\gamma L_1))\frac{a_{12}}{a_{11}} + (sinh(\gamma L_1))Z_0} \\ \underline{(n_{11}+cosh(\gamma L_1))\frac{a_{21}}{a_{11}} + (sinh(\gamma L_1))\frac{1}{Z_0}} & (n_{21})\frac{a_{12}}{a_{11}} + (Z_0\sin h(\gamma L_1))\frac{a_{21}}{a_{11}} \end{pmatrix}, \tag{4a}$$

$$\begin{pmatrix} p_{11} & p_{12} \\ p_{21} & p_{22} \end{pmatrix}\begin{pmatrix} a_{11} & a_{12} \\ a_{21} & a_{11} \end{pmatrix}^{-1} = \begin{pmatrix} a_{11} & a_{12} \\ a_{21} & a_{11} \end{pmatrix}\begin{pmatrix} \cos h(\gamma L_2) & Z_0\sin h(\gamma L_2) \\ \frac{1}{Z_0}\sin h(\gamma L_2) & \cos h(\gamma L_2) \end{pmatrix}, \tag{5}$$

$$\begin{pmatrix} p_{11}-\cos h(\gamma L_2) & \underline{p_{12}} \\ \underline{p_{21}} & p_{11}-\cos h(\gamma L_2) \end{pmatrix}$$

$$= \begin{pmatrix} (p_{12})\frac{a_{21}}{a_{11}} + \left(\frac{1}{Z_0}\sin h(\gamma L_2)\right)\frac{a_{12}}{a_{11}} & \underline{(p_{11}+\cos h(\gamma L_2))\frac{a_{12}}{a_{11}} + (\sin h(\gamma L_1))Z_0} \\ \underline{(p_{11}+\cos h(\gamma L_2))\frac{a_{21}}{a_{11}} + (\sin h(\gamma L_2))\frac{1}{Z_0}} & (p_{21})\frac{a_{12}}{a_{11}} + (Z_0\sin h(\gamma L_1))\frac{a_{21}}{a_{11}} \end{pmatrix}. \tag{5a}$$

where $n_{i,j}$ and $p_{i,j}$ are the elements of the ABCD matrix relating to the measured line 1 and 2, respectively.

The underline terms in (4.a) and (5.a) are common terms that generate two simultaneous equations allowing computation of Z_0 and the ratios a_{12}/a_{11} and a_{21}/a_{11} as:

$$Z_0 = \frac{p_{12}(\cos h(\gamma L_1)+m_{11}) - m_{12}(\cos h(\gamma L_2)+p_{11})}{(m_{11}+\cos h(\gamma L_1))\sin h(\gamma L_2) - (p_{11}+\cos h(\gamma L_2))\sin h(\gamma L_1)}, \tag{6}$$

$$\frac{a_{12}}{a_{11}} = \frac{n_{12}\sin h(\gamma L_2) - p_{12}\sin h(\gamma L_1)}{(m_{11}+\cos h(\gamma L_1))\sin h(\gamma L_2) - (p_{11}+\cos h(\gamma L_2))\sin h(\gamma L_1)}, \tag{7}$$

$$\frac{a_{21}}{a_{11}} = \frac{n_{21}(\sin h(\gamma L_2)) - p_{21}\sin h(\gamma L_1)}{(m_{11}+\cos h(\gamma L_1))\sin h(\gamma L_2) - (p_{11}+\cos h(\gamma L_2))\sin h(\gamma L_1)}. \tag{8}$$

Notice that (6)-(8) depends on γ, however, in Ref. 17 was reported a procedure to determine it, based on the measurement of two lines and using wave cascade formalism. Moreover, a_{11} is determined by taking into account symmetrical and reciprocal properties, in which the determinant of $[M_{Pad}]$ has to be equal to 1, this fact allows the computation of a_{11} as follows

$$a_{11}^2 = \frac{m_{11}+(\cos h(\gamma L_1))\sin h(\gamma L_2) - (p_{11}+\cos h(\gamma L_2))\sin h(\gamma L_1)}{2\sin h(\gamma(L_1-L_2))}. \tag{9}$$

Note that the analytical expression for calculating Z_0, a_{12}, a_{21} and a_{11} depends on γ and the physical lengths of L_1 and L_2. The propagation constant is determined using the two lines method reported in Ref. 17. The knowledge of Z_0, a_{11}, a_{12}, and a_{21} allows the calculation of $[M_{Pad}]$ and $[M_L]$. Several measurements at different landing positions of the probe tips showed repeatability in the S-parameters measurements of the lines as well as the computation of Z_0, a_{12}, a_{21} and a_{11} and γ. Errors could arise when the position of the probe tips change, but this is expected at very high frequencies ($>$ 110 GHz) when the maximum dimension of the pad is larger than λ/20. In our case at the maximum frequency of operation (20 GHz), the maximum dimension of the pad is smaller than λ/20 and therefore it can be considered as lumped element. The critical point here is to guarantee a good contact of the probe tips to the pads.

Another advantage that the L-L method offers, is that allows the accurately determination of an electrical equivalent circuit (EEC) of the CMOS pads. The CMOS pads used in this work were optimized to achieve higher operation frequencies because the available fabrication process only uses three metallization layers. The cross section view of the pad is shown in Fig. 2a. The EEC can be obtained by trans-

forming the ABCD matrix of the pad ($[M_{Pad}]$) into its Z-parameters matrix. Then using a T-network, as shown in Fig. 2b, along with the Z-parameters representation, the value of the element of the EEC can be computed directly.

The proposed method differs completely from [18] in two issues, which are the circuit for modeling the pads and the procedure to determine the line impedance. In Ref. 18 the EEC of the pad is modeled with shunt admittance (Y_L) approach and it is determined from the measured Y-parameters of two uniform transmission lines, without the knowledge of γ and Z_0. Since transmission lines are symmetric, swapping property can be applied, this means that swapping the ports 1 and 2 yields to the same matrix. Then according to the procedure described in Ref. 18, Y_L can be computed as:

$$\begin{pmatrix} Y_L & 0 \\ 0 & -Y_L \end{pmatrix} = \frac{Y_{LT} - Swap(Y_{LT})}{2} \quad (10)$$

where Y_{LT} is the Y-parameters matrix of a line with length $L_2 - L_1$, which is computed from the measurements of the line two, with line one in terms of ABCD matrix parameters.

3. Experimental Results

Using a standard CMOS 0.5μm fabrication process several transmission lines of different lengths, dummy structures (open, short, pads) and CMOS FETs embedded in pad structure as showed in Fig. 1, were fabricated in a die area of 16 mm^2. Moreover, the PNA-X (N5242A) was calibrated with the SOLT technique using the CS-5 calibration standard. All the measurements were taken at the center of the pads.

By using the measurements of two uniform lines of different length but equal arbitrary characteristic impedance, the propagation constant γ and the characteristic impedance (Z_0) were computed according to [19]. Notice that at this point, the pads are considered *black boxes*. Now applying (7)-(9), the elements of the ABCD matrix of $[M_{pad}]$ are determined. Then the EEC of the pad can be determined converting $[M_{pad}]$ into Z-parameters and by using a T-network. Figure 2 shows the values of the element of the EEC. Notice that the EEC of the pad is completely different to the one used in Ref. 8. In addition, it was demonstrated that, for the technology used in this work, the representation of the pads by a symmetrical and reciprocal ABCD matrix along with the use of two uniform lines allowed us the determination of a more accurate EEC model of the CMOS pads, since the resistances R_1, R_2 and R_3 shown in Fig. 2 cannot be determined with the procedure described in Ref. 8.

To show the inaccuracy of a simple shunt admittance to model the CMOS pads, Fig. 3 shows the Z_0 of the line, computed with [8] and with the proposed EEC of the CMOS pads. Notice that when [8] is used, the real part of Z_0 shows dispersion at frequencies above 2 GHz while the real part of Z_0 determined with the proposed de-embedded method shows a more constant behavior. This fact can be attributed to the

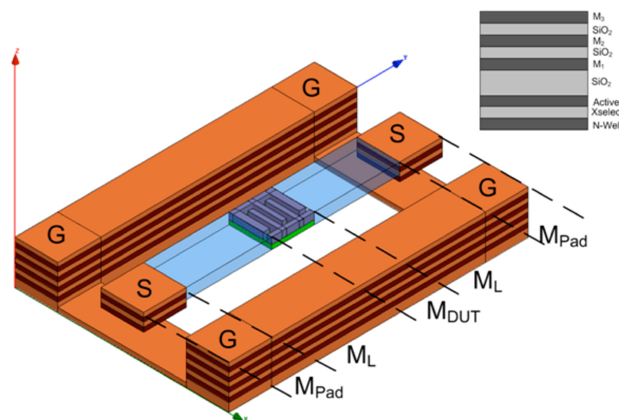
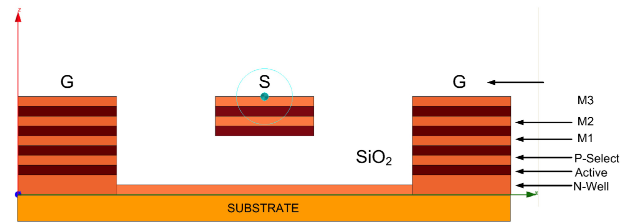
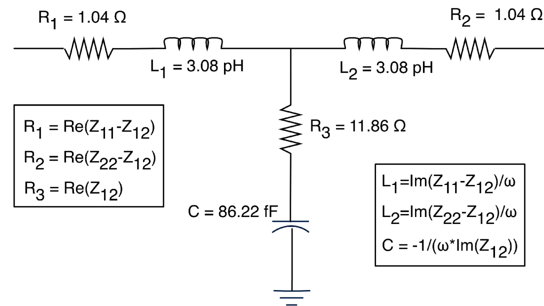


FIGURE 1. Structure of the on-wafer CMOS FET.



(a)



(b)

FIGURE 2. Pad structure used in this work: a) Cross section view of the structure used for the fabrication of the CMOS pads; b) Proposed electrical equivalent circuit.

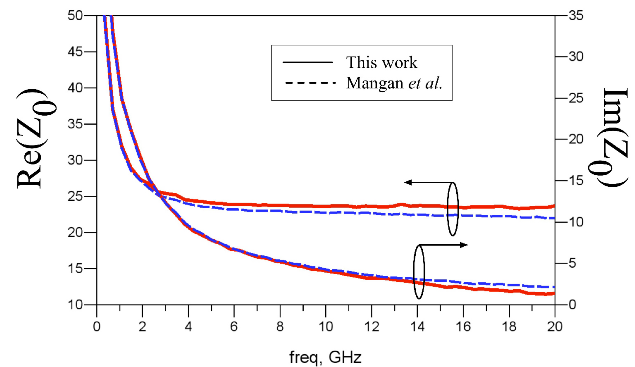
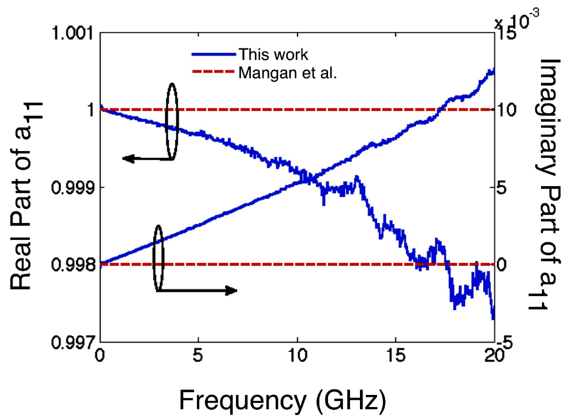
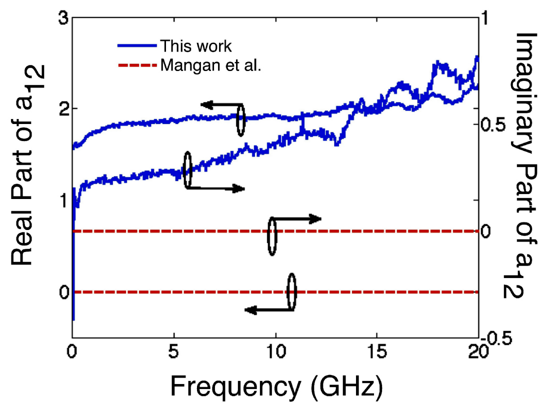


FIGURE 3. Characteristic impedance of a line computed by using the L-L and the Mangan method.



(a)



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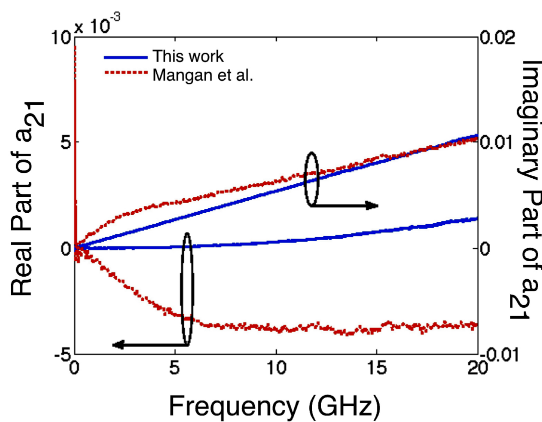
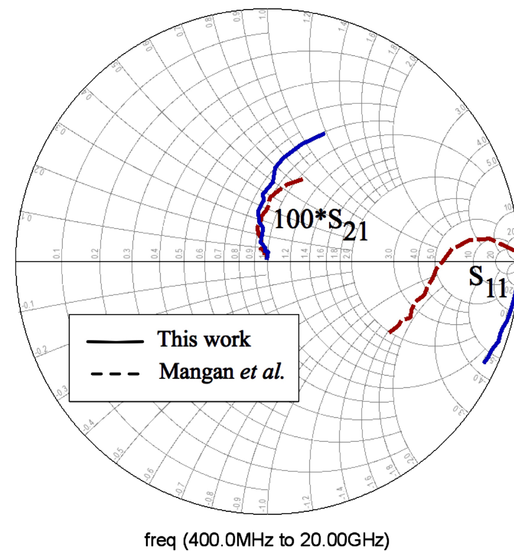
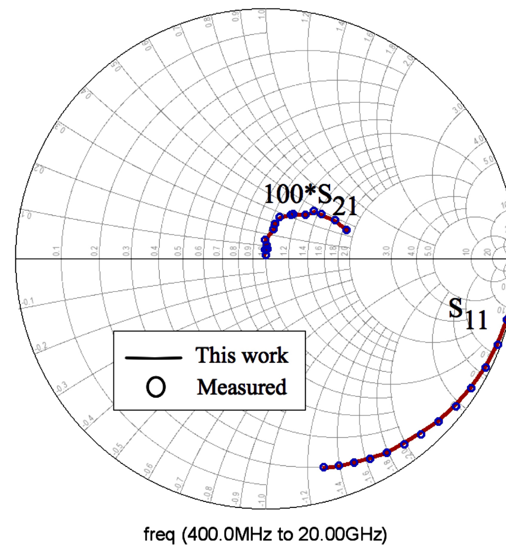


(c)

FIGURE 4. Real and imaginary parts of [M_{Pad}]: a) real and imaginary parts of a_{11}; b) real and imaginary parts of a_{12}; c) real and imaginary parts of a_{21}.



(a)



(b)

FIGURE 5. Open dummy structure: a) De-embedded S-parameters of an open dummy structure; b) Measured and simulated data of an open dummy structure using the proposed EEC of the pad.

model of the pads, and is verified in Fig. 4, in which the real and imaginary part of $[M_{Pad}]$ are compared with the ABCD matrix of a simple shunt admittance, computed with the method reported in Ref. 8 and [18]. The results show a significant difference in the a_{12} term and also in the real part of a_{21}, that indicates a negative conductance.

Now to verify whether a shunt admittance approach can be used as an EEC of the CMOS pad, de-embedded S-parameters data of an open dummy structure was used to reproduce the original measurement, this means an open embedded in interconnection lines and pads.

Figure 5a shows the de-embedded S-parameters using [8] and the proposed pad model. Note that the de-embedded S_{11} using [8] differs completely from an open circuit behavior. Figure 5b compares the measured open dummy structure with

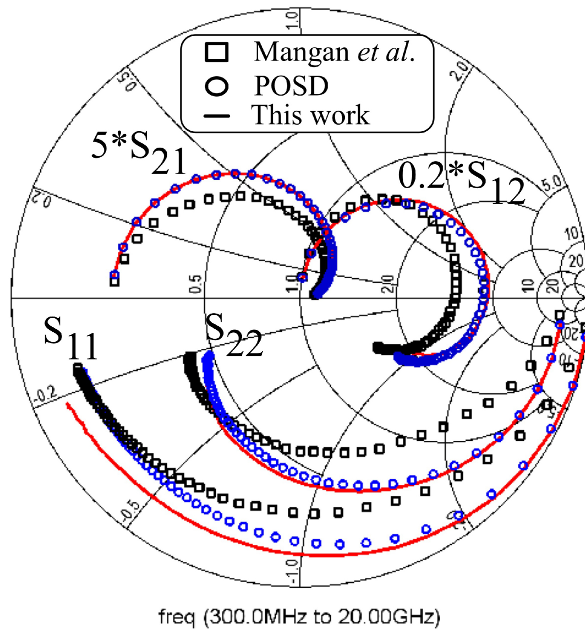


FIGURE 6. CMOS FET de-embedded at V_{GS} = 2.8 V and V_{DS} = 4.8 V using [4], PSOD and the proposed method.

simulated data (EEC of the pad with the de-embedded open dummy structure). This result shows a high correlation between the measured and the simulation data.

To perform the de-embedding of the open structure, the pads were represented as ABCD matrices; this means that in the case of [8] the real part of the shunt admittance was considered negative as shown in Fig. 4c. Moreover, the respective characteristic impedances and γ of the lines were computed according to the procedure described in Ref. 8 and using our proposed method. Then the respective EEC of the pads were used, in the case of [8] the EEC of the CMOS pad is a shunt capacitance of 4.9 pF, theoretically this shunt capacitance should represent the CMOS pads, as suggested in Ref. 12. However, Fig. 5b, demonstrates clearly that a simple shunt admittance approach does not suffice to accurately model the CMOS pads.

Figure 6 shows the de-embedding result of a CMOS FET embedded in two lines of 54μm and pads. The de-embedding was performed using the PSOD method, the Mangan method [8] and the proposed EEC of the pad. This result demonstrates that the PSOD converge with the method using the EEC of the pad. However, there is a little discrepancy between the PSOD and the proposed EEC, but this fact is attributed to the quality of the standards used in the PSOD, since high reflecting coefficient standards (open or short) is very difficult to achieved in a broadband frequency range (see Fig. 5b).

4. Conclusion

A fast and simple de-embedding method suitable for on wafer CMOS FETs has been presented. The method uses two uniform lines of different lengths but with the same characteristic impedance. Moreover, the method offers the possibility of accurately determine the CMOS pads parameters used to model them by means of an electrical equivalent circuit (EEC). Thus, our results demonstrate that a simple shunt admittance approach cannot be used to accurately model the CMOS pads. Despite its simplicity, the results from the proposed de-embedding method agree with the most popular de-embedding technique (PSOD). The proposed method reduces the cost of fabrication since dummies structures are no longer necessary.

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