Long-term reliability analysis of bipolar stress in SiC power MOSFETs

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This paper examines the reliability of SiC DMOS power transistors in a DC-DC boost converter circuit. This reliability analysis focuses on the impact of bias temperature instabilities (BTI) on the electrical performance of the transistor, taking into account the variation of one of the most critical parameters of a SiC power MOSFET: the on-resistance ($R_{\rm on}$). The study presented in this work also provides an insight into the importance of using an accurate physical reliability model to estimate the transistor's real threshold voltage drift for a long operating time. We demonstrate that SiC DMOS technology exhibits a higher threshold voltage ($V_{\rm th}$) and $R_{\rm on}$ stability when operated in a bipolar mode. As a result, data derived from measure-stress-measure (MSM) sequences are used to calibrate the defect parameters of a two-state non-radiative multi-phonon model (NMP) that captures the charge trapping kinetics of oxide and interface defects in a reliability simulation framework, Comphy. The analysis shows that an extrapolation of device deterioration at operating conditionssettings reduces bias temperature instabilities (BTI), leading to a minimal on-state loss degradation.

Keywords: Reliability; charge trapping; bias temperature instabilities; on-resistance.

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1. Introduction

Power converter circuits are widely used in many applications where their continuous operation is required. However, these converters are continuously under stressful conditions like overvoltage, overcurrent, high temperature, and harsh environments, which leads to an unavoidable degradation of the components of the circuit, causing, in some cases, irreversible damage. In real operating conditions, power devices are frequently subjected to coupled thermo-mechanical and electrical stresses, such as those induced by power cycling, which can simultaneously affect both chip-level and package-level reliability. These conditions have been shown to induce progressive degradation in key parameters such as threshold voltage, on-state resistance, and switching performance, ultimately impacting device lifetime and system reliability [1].

Under high switching speeds and voltage slew rates, additional dynamic stress mechanisms may arise, further challenging device reliability [2]. In addition to long-term aging mechanisms, recent studies have shown that extreme operating conditions such as short-circuit events and high electrical stress can significantly accelerate degradation processes and trigger failure mechanisms such as gate oxide breakdown and thermal runaway, severely impacting device reliability [3].

In this sense, power semiconductor switches are well known to be the most affected and, hence, the main cause for the system failure [4, 5]. Some reports and studies indicate that almost a third of the total failure is due to the aging phenomena of semiconductor switches, which are generally MOSFET transistors [6]. With the integration of wide-bandgap materials, such as SiC, it has been possible to design more efficient power electronics systems. This material exhibits notable advantages in terms of electrical breakdown field, thermal conductivity, and high electron mobility [7], which result in lower on-resistance ($R_{\rm on}$) values than conventional silicon technology.

However, it is well known that the bias temperature instabilities (BTI) degradation phenomena for SiC MOSFETs may lead to thermal stress of the device, a decrease in efficiency, electrical stress at the gate area, an increase of the transistor leakage current due to breakdown, as well as an increase of the $R_{\rm on}$ and other undesirable effects [8–13]. Recent works have highlighted that extreme electric field stress can activate additional degradation pathways, such as hole injection and trap generation in the gate oxide, which significantly accelerate threshold voltage instability [14].

One crucial aspect to be considered for the SiC power MOSFETs, precisely, is the threshold voltage drift ($\Delta V_{\rm th}$) under long-term operation. The BTI impact caused by continuous bias at the gate has been well studied [15–20]. However, recent studies have shown that the degradation behavior of SiC MOSFETs strongly depends on the device structure, particularly in trench gate configurations, where electric field crowding and oxide/interface quality can lead to significantly different reliability characteristics compared to planar devices. In particular, distinct threshold voltage instability mechanisms, including electron and hole trapping, have been reported to vary with gate architecture, bias polarity, and temperature [21]. At the physical level, this degradation is mainly attributed to charge trapping and detrapping processes associated with defects at the SiC/SiO2 interface and within the gate oxide, which govern the threshold voltage shift under both DC and AC stress conditions [22].

The different properties of the semiconductor-dielectric interface and the nature of the wide-bandgap material silicon carbide (SiC) compared to its silicon counterpart cause some peculiar characteristics in the $V_{\rm th}$ variation and BTI. On the other hand, while these SiC properties are suitable for circuit applications, the degradation of SiC MOSFETs under several operating conditions, including switching frequency, needs to be fully understood, especially under dynamic operating conditions where recent studies have reported complex interactions between gate bias, temperature, and switching cycles affecting threshold voltage stability [23]. In particular, recent studies have highlighted that conventional static stress tests are not sufficient to capture the complex degradation mechanisms occurring under dynamic high dV/dt conditions, where electric field enhancement and gate oxide stress can significantly impact device reliability [2] It could be beneficial to determine the useful lifetime of commercially introduced and available devices [24].

Another significant advantage of the commercially SiC power transistors is the switching-speed performance (speed between on and off states), where a $R_{\rm on}$ as low as possible is required [25]. However, $R_{\rm on}$ is significantly influenced by the driving voltage, *i.e.*, the gate voltage. Therefore, to know how the $R_{\rm on}$ behaves under the instabilities introduced by the gate voltage stress, the reliability study of power MOSFETs based on SiC gains more critical importance.

The threshold voltage of SiC power MOSFETs, besides the drift caused by static stress, may undergo an additional shift triggered by switching events (turn-On and turn-Off of the transistor). Under more extreme operating conditions, such as high-amplitude gate voltage transients or electrostatic discharge-like events, the degradation can be further accelerated due to strong electric field effects in the gate oxide. Recent studies have shown that hole trapping and field-assisted charge injection dominate the threshold voltage instability under such ultra-high gate stress conditions, leading to significant $V_{\rm th}$ shifts and oxide degradation [14]. It is only possible to identify this other component in long-term switching tests. Recent studies have shown that under dynamic gate stress conditions, this threshold voltage drift can be significantly enhanced and is strongly dependent on operating conditions such as temperature and gate bias, directly impacting on-resistance and long-term device reliability [22]. The effect is related to gate-oxide trap dynamics [12, 26]. The increase of $V_{\rm th}$ causes a slight rise in $R_{\rm on}$, which translates into increased on-state losses over time. For this reason, to account for a very accurate physical trapping model to predict the $V_{\rm th}$ drift behavior over time, it is essential to consider defect-dependent charge trapping mechanisms at the atomic scale, which directly influence the long-term instability of SiC MOSFETs [22], as well as degradation under cyclic electrothermal stress conditions, where the interaction between static and dynamic degradation mechanisms significantly influences long-term device reliability and lifetime prediction [1].

Finally, in this work, we highlight the importance of using a very accurate physical defect model to estimate the threshold voltage drift ($\Delta V_{\rm th}$) over time. We also present the remarkable difference when the transistors work under bipolar $V_{\rm G}$ operation and unipolar $V_{\rm G}$ operation in terms of $R_{\rm on}$ variation due to the impact of the BTI degradation mechanism, which is critical for the lifetime projection operation of the devices.

2. Stress pattern definition and physical charge trapping model calibration

SiC DMOSFETs commonly use a bipolar gate drive, where a slightly negative voltage is applied during the off-state. This technique helps suppress long-term changes in both $V_{\rm th}$ and $R_{\rm on}$, which are typically affected by BTI.

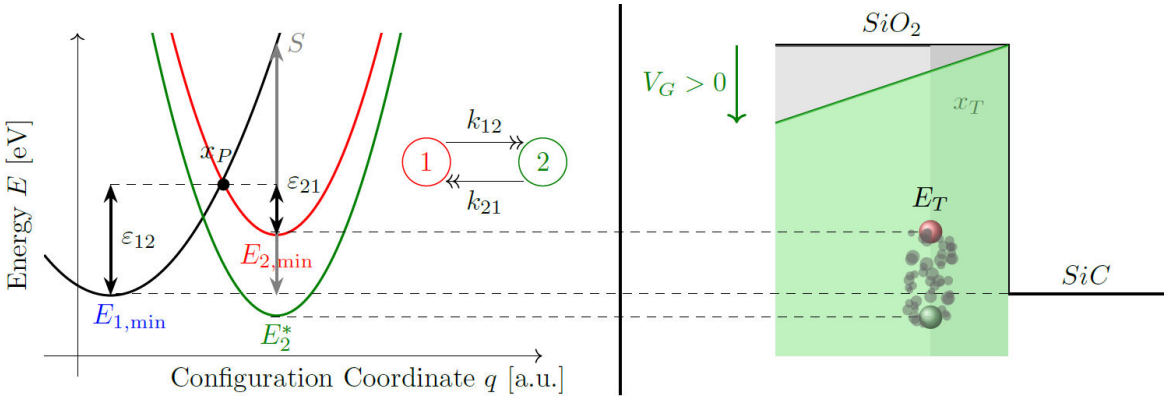

FIGURE 1. Configuration coordinate diagram illustrating the two-state non-radiative multi-phonon (NMP) model for oxide defects. The potential energy surfaces E_1(q) and E_2(q) represent the defect in two different charge states as a function of the configuration coordinate q. Transitions between states, governed by phonon-assisted capture and emission rates $k_{\rm ij}$, depend on the energy barriers E_{12} and E_{21}. The diagram includes alignment of defect levels relative to the conduction band edge $E_{\rm C}$, valence band edge $E_{\rm V}$, and trap level $E_{\rm T}$. This model is used within the Comphy simulation framework to evaluate the occupancy dynamics of defects over time, which directly influence the effective threshold voltage shift ($\Delta V_{\rm th}$) observed in BTI-stressed MOSFETs.

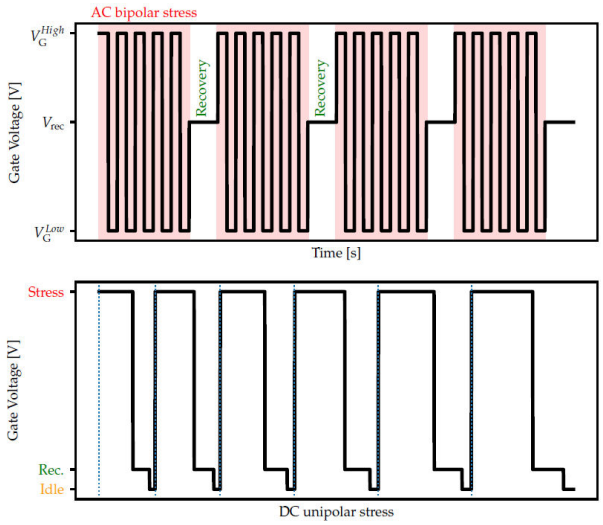

FIGURE 2. AC (top) and extended DC (bottom) MSM stress schemes are used to extract threshold voltage shift (ΔV_{th}) over time. The AC scheme applies pulsed gate stress with recovery, while the DC scheme uses prolonged stress phases to capture long-term degradation behavior in SiC MOSFETs.

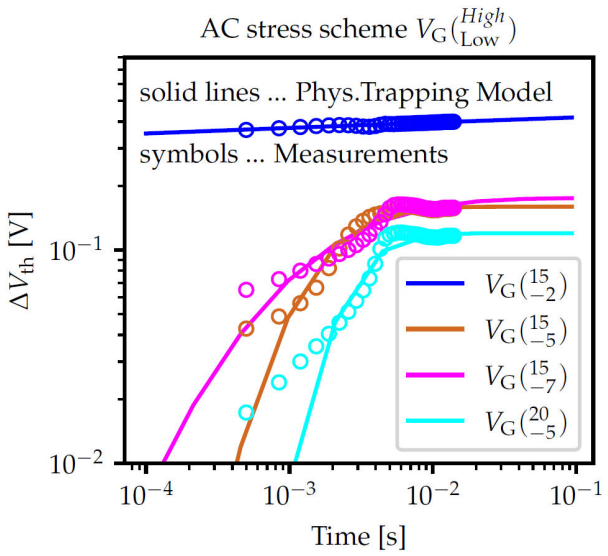

FIGURE 3. Experimental threshold voltage drift values can be reproduced accurately by using the Comphy reliability simulator based on the Physical Charge Trapping Model (NMP) for an AC MSM scheme.

BTI is mainly caused by charge trapping at defects near the interface between the channel and gate oxide. To analyze and predict this behavior, researchers use a non-radiative multi-phonon (NMP), as depicted in Fig. 1, which is based on detailed physical parameters of the materials and defects involved.

To accurately model the charge trapping behavior of oxide and interface defects, we calibrate a two-state non-radiative multi-phonon model within our simulation framework, Comphy [26]. This calibration is based on experimental data derived from measure-stress-measure (MSM)

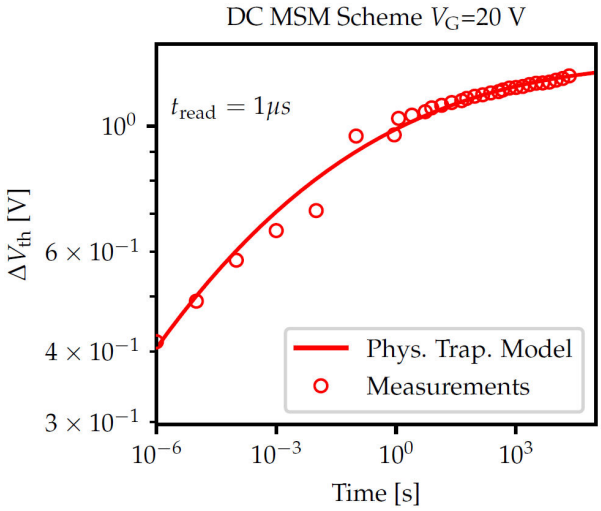

FIGURE 4. Experimental threshold voltage drift values can be reproduced accurately by using the Comphy reliability simulator based on the Physical Charge Trapping Model (NMP) for a DC MSM scheme.

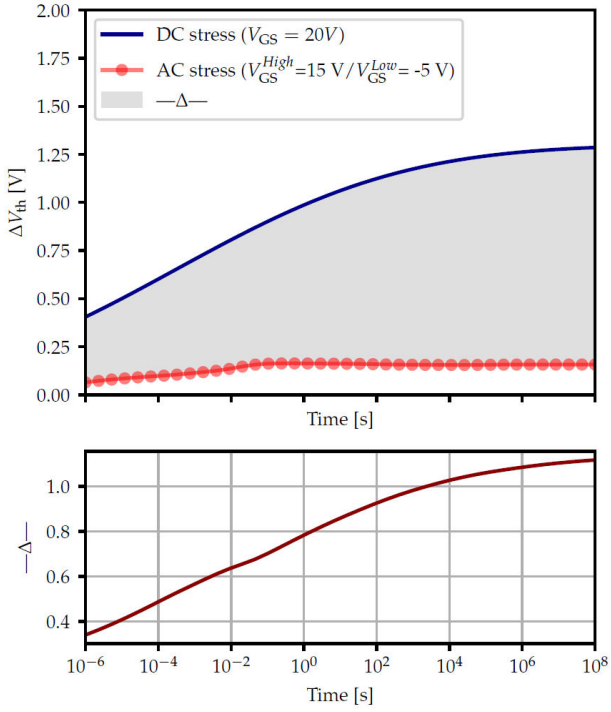

FIGURE 5. Threshold voltage shift (ΔV_{th}) over time under AC and DC stress, extrapolated up to 10 years after calibrating the reliability simulation framework, highlighting stronger degradation from constant high-voltage DC stress compared to pulsed AC stress conditions.

sequences, which provide insights into the underlying defect dynamics. A comprehensive dataset collected from a commercially available SiC DMOSFET, which includes both long-term DC stress and short-term AC MSM (measure-stress-measure) sequences, as shown in Fig. 2, is utilized to extract the characteristics of the underlying defects.

TABLE I. Boost converter circuit parameters.

Parameter	Value
$V_{\rm in}$	400 V
$V_{\rm out}$	800 V
$f_{\rm sw}$	100 kHz
$I_{\rm in}$	6.18 A
$V_{\rm GS}$	(PWM) $+15/-4$
C	20.15 μF
$P_{\rm out}$	2600 W

The results of both short-term AC $V_{\rm th}$ data for bipolar gate drive and long-term DC $V_{\rm th}$ data for accelerated $V_{\rm G}$ at $T = 300$ K stress situations and standard operating circumstances are displayed in Figs. 3 and 4, respectively. As can be seen, the physical charge trapping model (NMP) accurately reproduces the observed behavior of $\Delta V_{\rm th}$ for both stress conditions. This allows the calibration of our simulation framework to reproduce the $\Delta V_{\rm th}$ behavior for extended operating times, for instance, up to 10 years. Simulation results show that bipolar gate operation significantly improves reliability and reduces degradation, making it possible to maintain stable performance with minimal efficiency loss even over extended lifetimes, such as 10 years, as shown in Fig. 5.

3. Analyzed circuit and reliability analysis strategy through SPICE simulation

Figure 6 shows the schematic representation of the DC-DC boost converter circuit analyzed in this work. The value of a typical operating frequency for SiC devices is 100 kHz, a duty cycle of 0.5, and $V_{\rm High}$ and $V_{\rm Low}$ of 15 V and -4 V, respectively, for the PWM pulse applied to the gate of transistors.

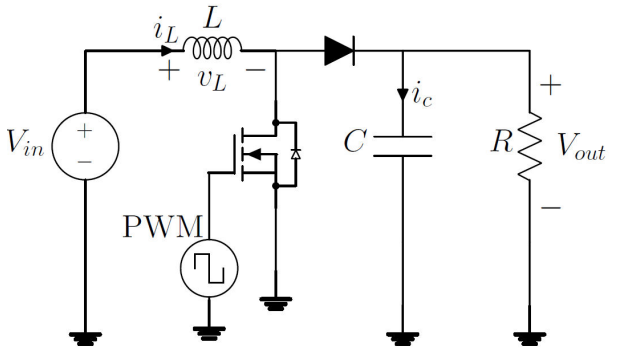

FIGURE 6. Schematic of the boost converter circuit analyzed in this work.

In this study, we used a commercially available SiC power MOSFET produced by Wolfspeed. To improve the accuracy of our analysis, we utilized the manufacturer-provided SPICE model. For engineers developing silicon carbide (SiC) power systems, Wolfspeed's SPICE models offer significant advantages, particularly in achieving accurate simulations and optimizing overall system performance. These models account for critical parasitic components-such as capacitances and inductances-that are vital for the behavior of high-speed SiC devices. Including these effects in simulations leads to results that more closely reflect real-world performance. The results from the simulation analysis were obtained considering the circuit performance parameters shown in Table I.

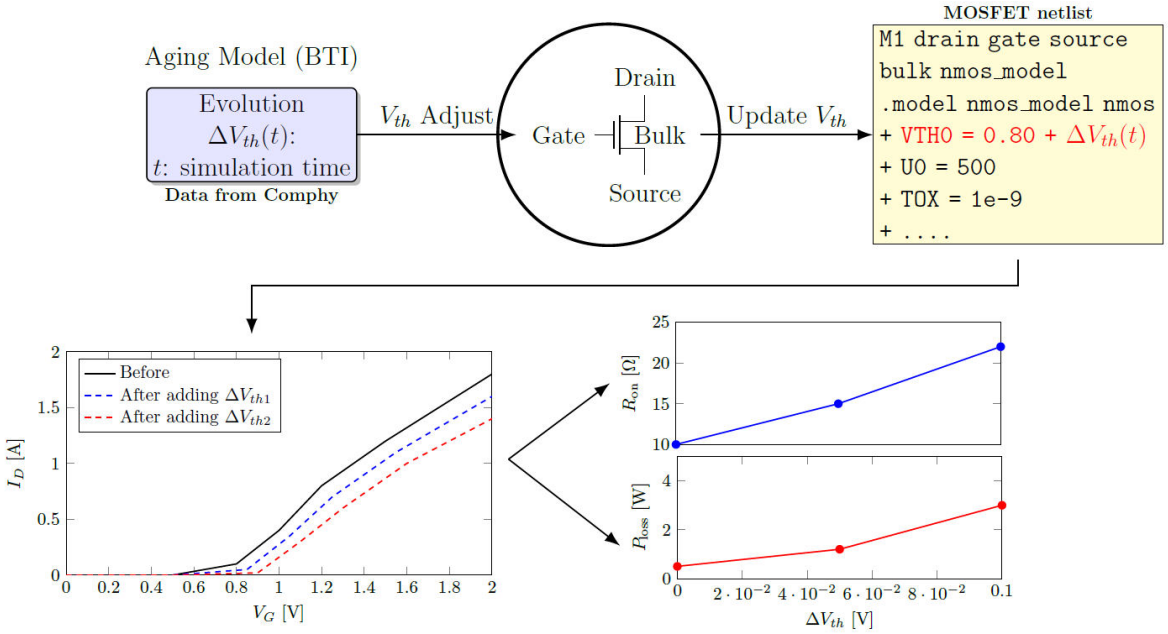

FIGURE 7. SPICE simulation of MOSFET aging using a BTI-induced threshold voltage shift model ($\Delta V_{\rm th}(t)$), integrated into the device netlist. The figure illustrates transfer characteristics, on-resistance ($R_{\rm on}$), and power loss evolution as $\Delta V_{\rm th}$ is updated over time.

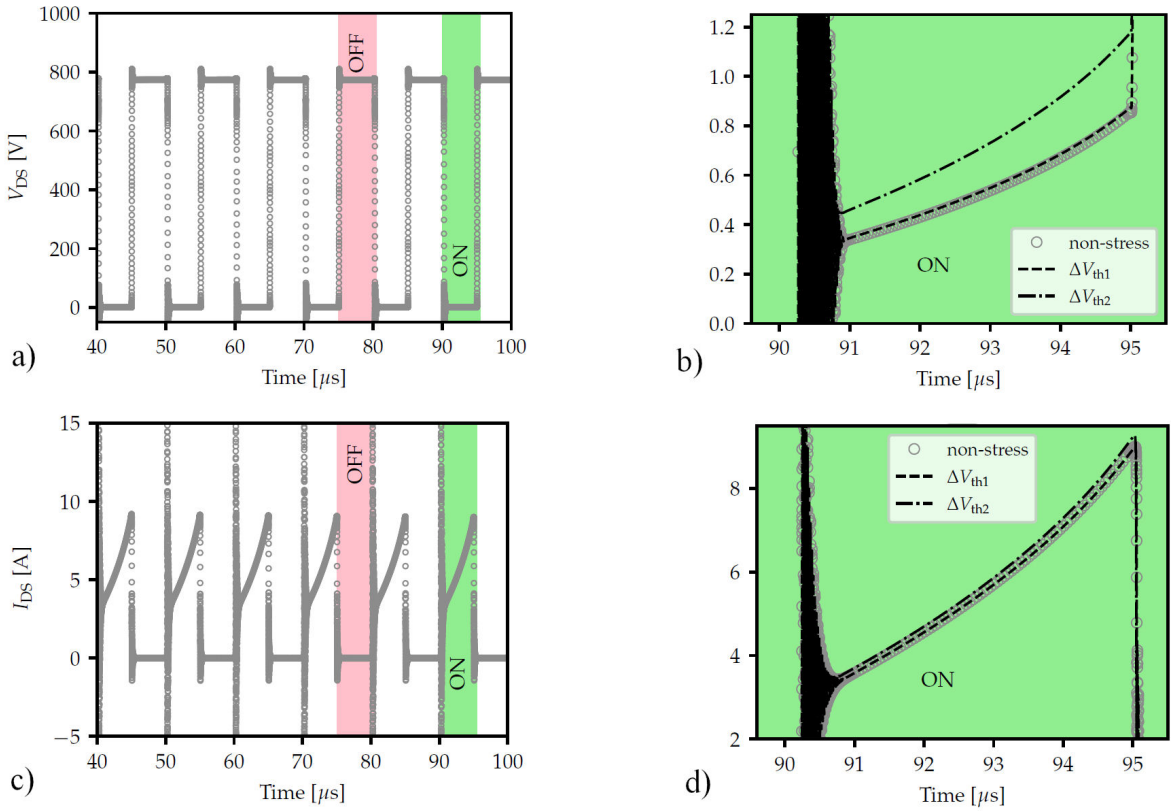

FIGURE 8. a) Drain-to-source voltage ($V_{\rm DS}$) and c) drain current ($I_{\rm DS}$) waveforms during switching events of boost converter circuit performance, illustrating ON and OFF states. b) Zoomed-in view highlighting the increase of $R_{\rm on}$ due to the rise of the $V_{\rm DS}$ minimum value when it drops during the ON state affected by the threshold voltage shift $\Delta V_{\rm th}$. d) $\Delta V_{\rm th}$ has negligible impact on $I_{\rm DS}$.

To represent the BTI impact on the transistor behavior, an equivalent modification is done to the netlist of the transistor model. It was considered adding an independent constant voltage source connected in series to the internal gate of the MOSFET to take into account the degradation of the device due to the known aging mechanisms, which means the drift of the threshold voltage ($\Delta V_{\rm th}$) [27,28], as shown in the diagram from Fig. 7.

Figure 8 shows the drain-to-source voltage ($V_{\rm DS}$) and drain-to-source current ($I_{\rm DS}$) during boost converter circuit performance. The extracted signals correspond to non-degraded operation conditions, *i.e.*, $\Delta V_{\rm th} = 0$, and consider degradation due to BTI impact for two different $\Delta V_{\rm th}$ values. As can be seen, BTI has a negligible impact on $I_{\rm DS}$. During on-state operating time, $V_{\rm DS}$ drops to a value close to zero due to an increase in the on-resistance caused by the threshold voltage drift ($\Delta V_{\rm th}$).

The increase in $V_{\rm DS}$ during the on-state suggests a progressive rise in $R_{\rm on}$, which can be linked to degradation of the channel region due to charge trapping at the $\rm SiC/SiO_2$ interface. This trapping modifies the inversion layer formation and reduces effective carrier mobility, thereby increasing the conduction resistance. Furthermore, additional contributions from contact resistance and package parasitics cannot be neglected under prolonged stress conditions.

On the other hand, the oscillations observed in the switching waveforms are primarily caused by the interaction between parasitic inductances in the circuit loop and the intrinsic capacitances of the device, forming an underdamped LC network. During fast switching transitions, this results in ringing phenomena in both voltage and current waveforms. The effect is further amplified by the high $\mathrm{d}v/\mathrm{d}t$ and $\mathrm{d}i/\mathrm{d}t$ characteristics of SiC MOSFETs, as well as the presence of packaging parasitics such as bond wire inductance. Therefore, these oscillations are mainly attributed to circuit-level parasitic effects rather than intrinsic device degradation mechanisms.

Using the well-known Ohm's law, the value $R_{\rm on}$ can be extracted as follows:

$$R_{\rm on} = \frac{V_{\rm DS-on}}{I_{\rm DS-on}}. \tag{1}$$

3.1. Impact of BTI on device and circuit parameters

In Fig. 9a), the computed parameter $R_{\rm on}$ extrapolation is presented for each $\Delta V_{\rm th}$ value over 10 years of operating time when both bipolar gate-drive and unipolar gate-drive operations are considered. Each $\Delta V_{\rm th}$ value contains singular degradation information at a specific time value during circuit performance.

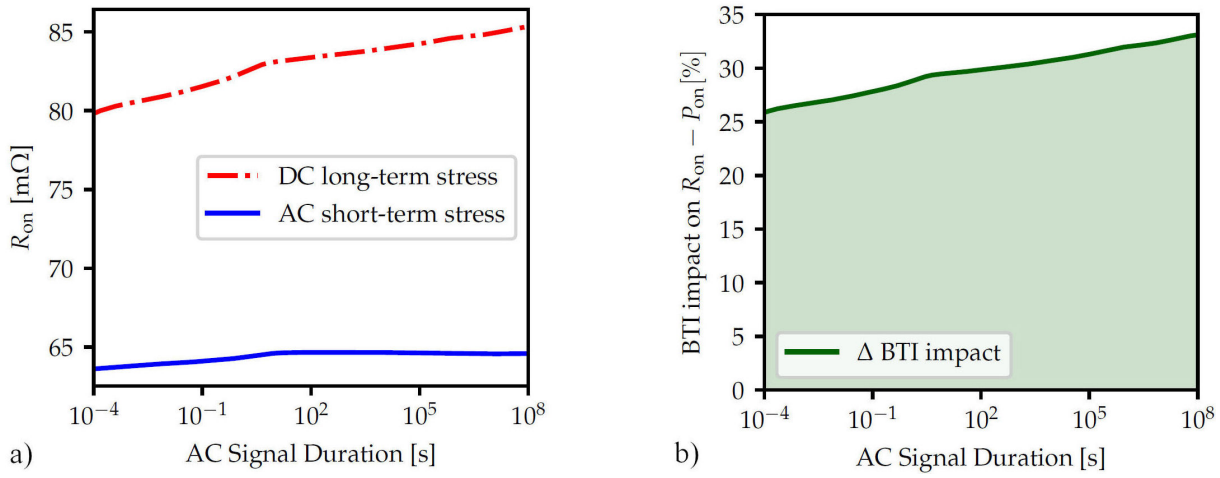

FIGURE 9. According to the extracted values of ΔR_{on} a) for each ΔV_{th} from our calibrated framework, static on-state losses after 10 years can be reduced around 30% when bipolar AC gate-drive operation is considered b).

It is noteworthy that, after a decade, the ΔR_{on} shows an increase of around 30% in on-state loss for unipolar gate-drive operation (long-term stress scheme) in comparison to bipolar AC mode (short-term stress scheme) at a duty cycle of d = 0.5, Fig. 9b). The higher gate stress in unipolar drive accelerates BTI degradation, leading to more pronounced shifts in device behavior. This degradation is particularly critical in high-frequency or high-load scenarios, where elevated R_{on} has a larger impact on converter performance. These findings highlight the importance of considering BTI effects during the design phase and suggest that gate-drive strategies should be carefully chosen to balance performance and long-term reliability.

4. Conclusions

In conclusion, our calibrated simulations estimate a 30% reduction in on-state loss at bipolar (AC) V_G operation over unipolar (DC) V_G gate-drive signals. According to these findings, BTI-induced degradation has only a minor impact to power conversion efficiency under the suggested operating circumstances. However, special attention has to be paid during the design phase for gate-driving strategies to mitigate BTI impact, especially in long-lifetime applications like automotive or industrial power converters.

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